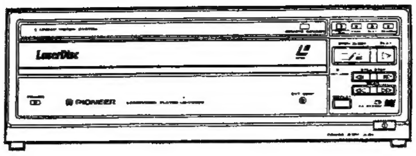
PIONEER®
The future of sound and vision.

Service Manual



ORDER NO.
ARP1758

LASERVISION PLAYER

LD-V8000

- This manual is applicable to the KUC type.
- For the circuit and mechanism descriptions, refer to the LD-V8000 service guide (ARP1759).

CONTENTS

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FI MAY 1989 Printed in Japan

1. SAFETY INFORMATION

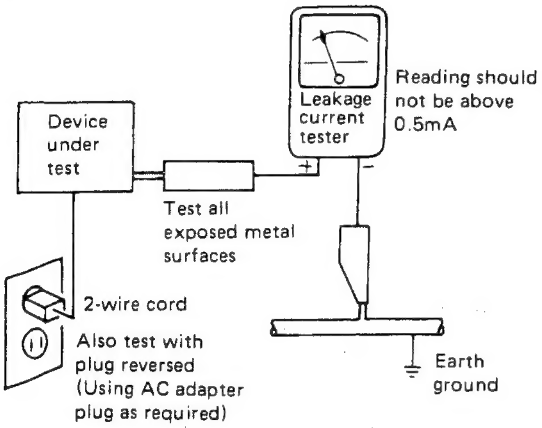
(FOR USA MODEL ONLY)

1. SAFETY PRECAUTIONS

The following check should be performed for the continued protection of the customer and service technician.

LEAKAGE CURRENT CHECK

Measure leakage current to a known earth ground (water pipe, conduit, etc.) by connecting a leakage current tester such as Simpson Model 229-2 or equivalent between the earth ground and all exposed metal parts of the appliance (input/output terminals, screwheads, metal overlays, control shaft, etc.). Plug the AC line cord of the appliance directly into a 120V AC 60Hz outlet and turn the AC power switch on. Any current measured must not exceed 0.5mA.



AC Leakage Test

ANY MEASUREMENTS NOT WITHIN THE LIMITS OUTLINED ABOVE ARE INDICATIVE OF A POTENTIAL SHOCK HAZARD AND MUST BE CORRECTED BEFORE RETURNING THE APPLIANCE TO THE CUSTOMER.

2. PRODUCT SAFETY NOTICE

Many electrical and mechanical parts in the appliance have special safety related characteristics. These are often not evident from visual inspection nor the protection afforded by them necessarily can be obtained by using replacement components rated for voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in this Service Manual.

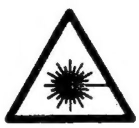
Electrical components having such features are identified by marking with a ⚠ on the schematics and on the parts list in this Service Manual.

The use of a substitute replacement component which does not have the same safety characteristics as the PIONEER recommended replacement one, shown in the parts list in this Service Manual, may create shock, fire, or other hazards.

Product Safety is continuously under review and new instructions are issued from time to time. For the latest information, always consult the current PIONEER Service Manual. A subscription to, or additional copies of, PIONEER Service Manual may be obtained at a nominal charge from PIONEER.

(FOR EUROPEAN MODEL ONLY)

VAROITUS!
LAITE SISÄLTÄÄ LASERDIODIN, JOKA LÄHETTÄÄ NÄKYMÄTÖNTÄ, SILMILLE VAARALLISTA INFRAPUNASÄTEILYÄ LAITTEEN SISÄLLÄ ON LASERDIODIN LÄHEISYYDESSÄ KUVAN 1. MUKAINEN VAROITUSMERKKI.

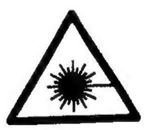


LASER
Kuva 1
Lasersateilyn varoitusmerkki

ADVERSEL:
USYNLIG LASERSTRÅLING VED ÅBNING NÅR SIKKERHEDSAFBRYDERE ER UDE AF FUNKTION UNDGÅ UDSAETTELSE FOR STRÅLING.

VIKTIGT
APARATEN INNEHÅLLER LASER AV HÖGRE KLASS ÄN 1. INGREPP I APPARATEN BÖR GÖRAS AV SPECIELLT UTBILDAD PERSONAL.

WARNING!
DEVICE INCLUDES LASER DIODE WHICH EMITS INVISIBLE INFRARED RADIATION WHICH IS DANGEROUS TO EYES. THERE IS A WARNING SIGN ACCORDING TO PICTURE 1 INSIDE THE DEVICE CLOSE TO THE LASER DIODE.

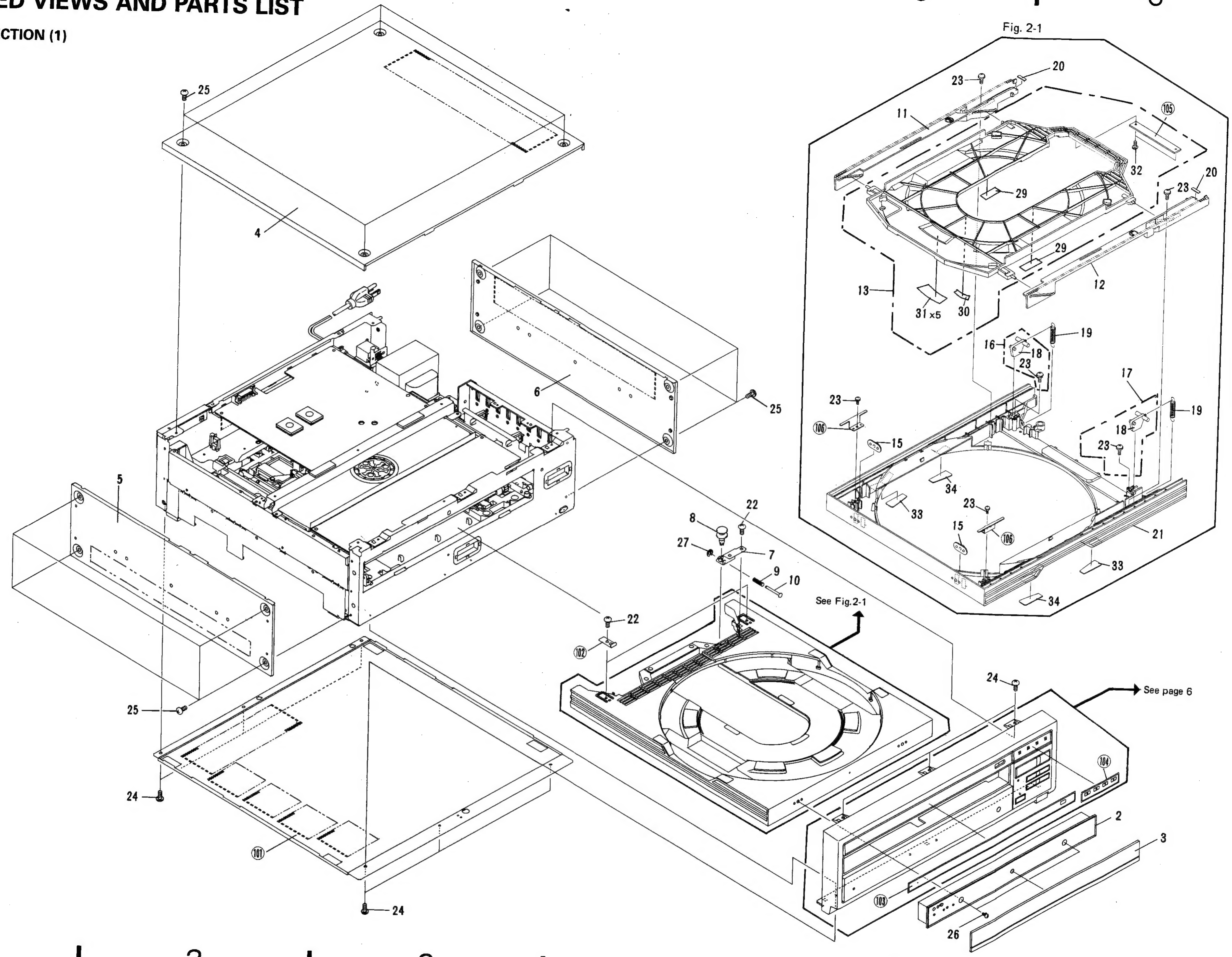


LASER
Picture 1
Warning sign for laser radiation

IMPORTANT
THIS PIONEER APPARATUS CONTAINS LASER OF HIGHER CLASS THAN 1. SERVICING OPERATION OF THE APPARATUS SHOULD BE DONE BY A SPECIALLY INSTRUCTED PERSON.

2. EXPLODED VIEWS AND PARTS LIST

2. 1 EXTERIOR SECTION (1)

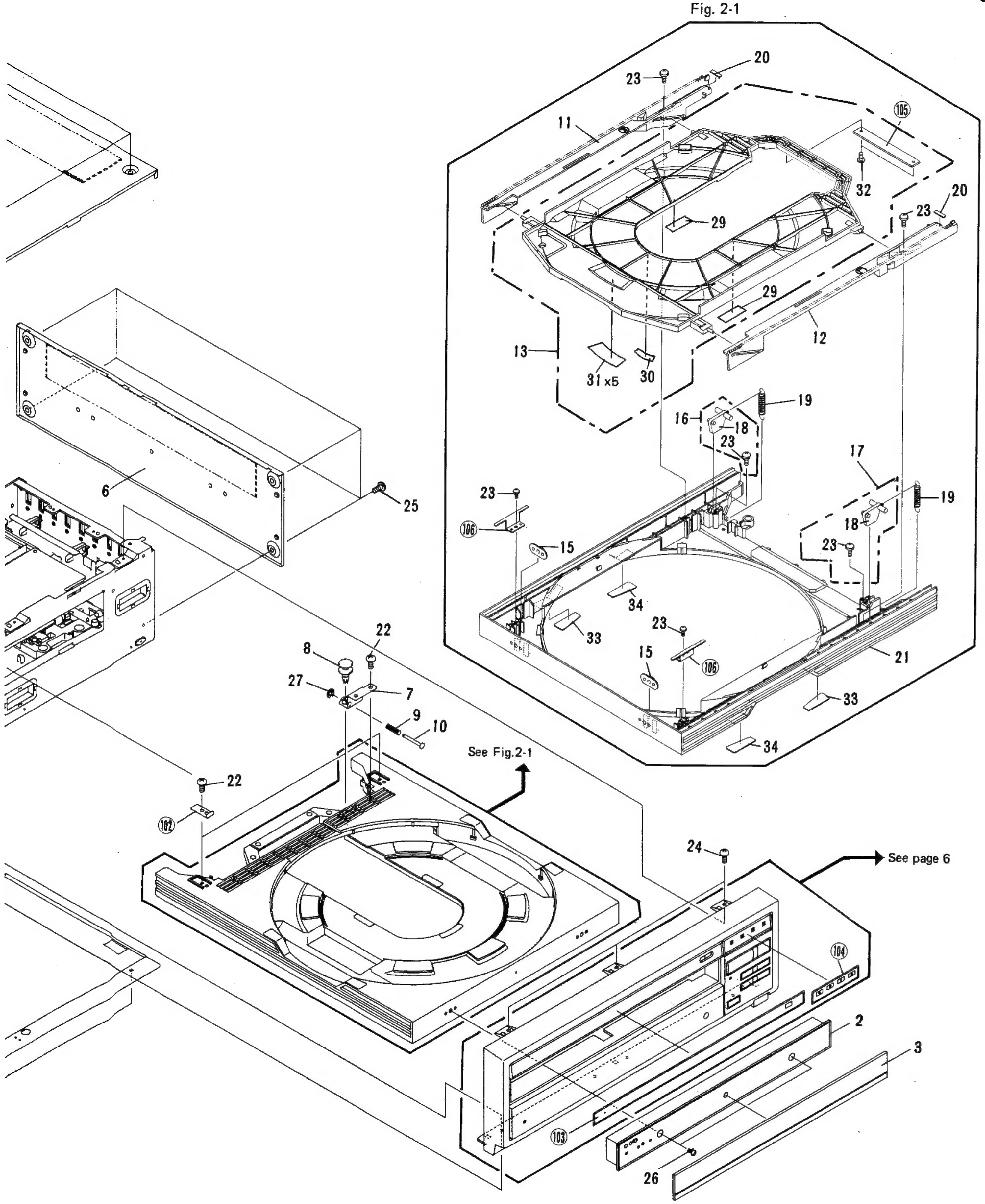


NOTE
- *Par*
- *The faci tion*
- *Par tha*

Parts

Mark

Fig. 2-1



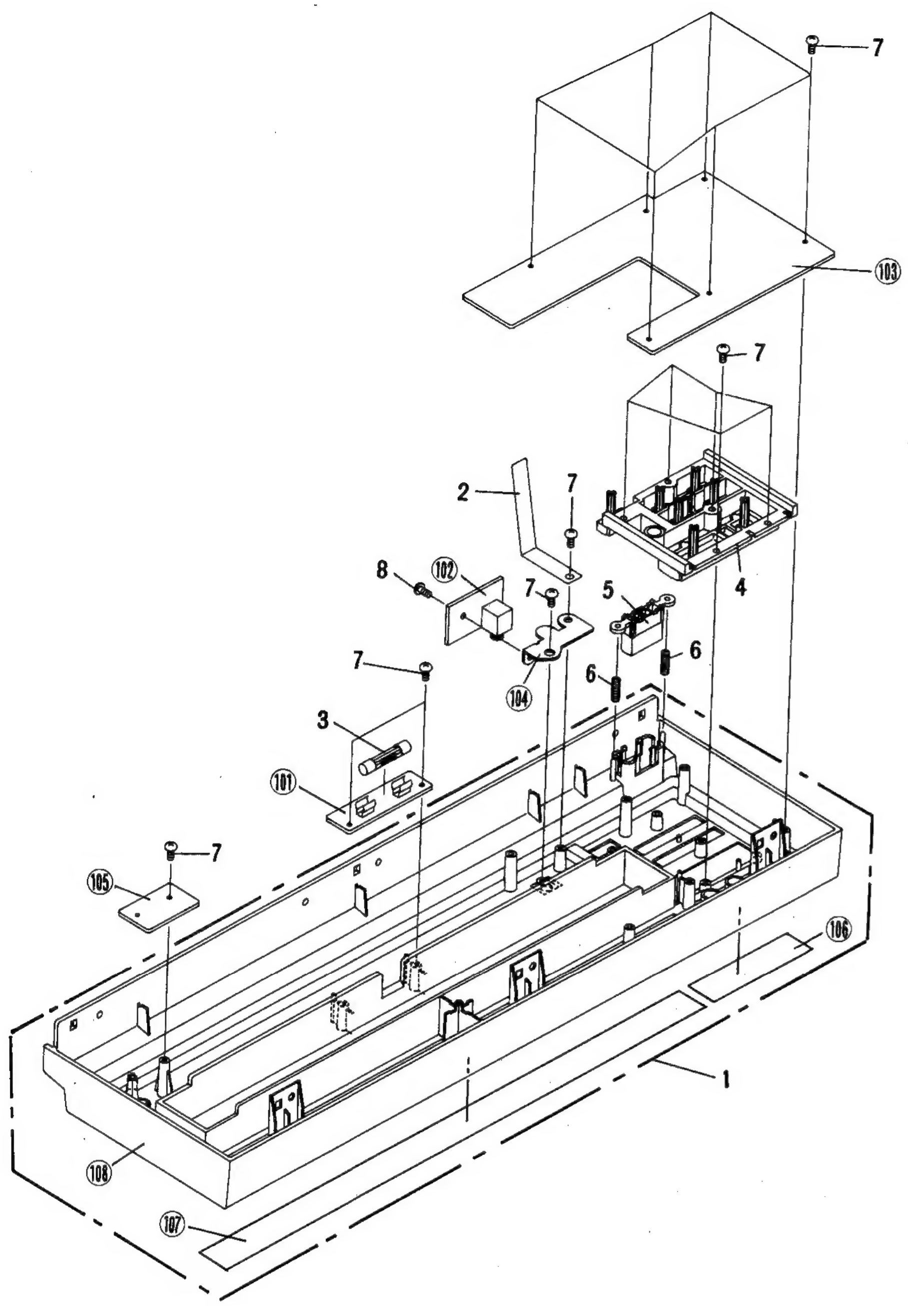
NOTES:
- *Parts without part number cannot be supplied.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*

Parts List of Exterior Section (1)

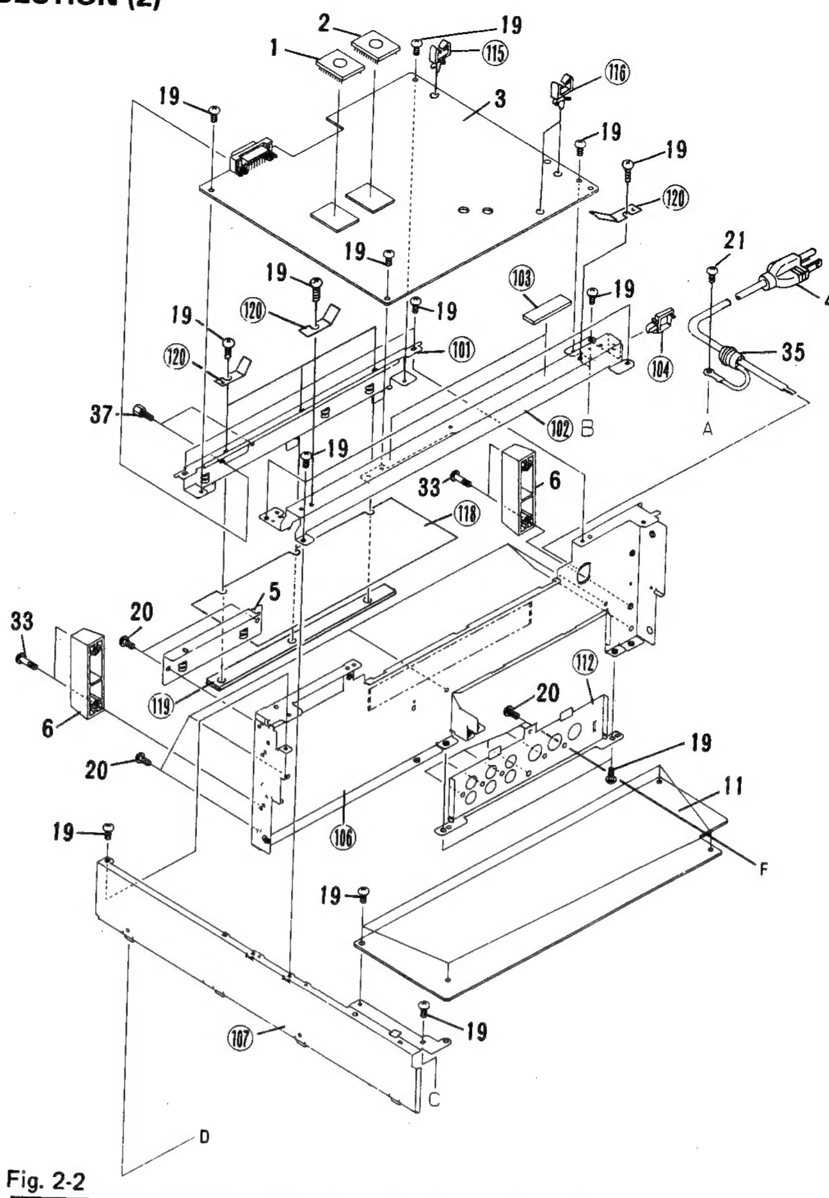
Mark	No.	Part No.	Description
	1.	. . .	. . .
	2.	DNK1159	Loading panel
	3.	DNK1330	Decoration panel
	4.	DNE1057	Top plate
	5.	DNE1066	Side panel
	6.	DNE1058	Side panel (L)
	7.	DXB1100	SW metal assembly
	8.	VEC1059	Prastic rivet
	9.	DBH1039	Spring
	10.	DLA1155	SW shaft
	11.	VNL1061	Rack gear (R)
	12.	VNL1060	Rack gear (L)
	13.	DXA1118	Container assembly
	14.	. . .	. . .
	15.	VBN-005	Nut
	16.	DXB1102	Stopper (R) assembly
	17.	DXB1101	Stopper (L) assembly
	18.	VNL1062	Stopper
	19.	VBH1021	Stopper spring
	20.	VEB1041	Rack dump rubber
	21.	DXA1117	Carry assembly
	22.	BPZ30P080FCU	Screw
	23.	IPZ30P080FCU	Screw
	24.	BBZ30P080FMC	Screw
	25.	FBT40P080FZK	Screw
	26.	PMA40P100FMC	Screw
	27.	YE20FUC	E-ring
	28.	. . .	. . .
	29.	DED1031	Disc pad B
	30.	DED1030	Disc pad A
	31.	DED1032	Disc pad C
	32.	BPZ30P060FMC	Screw
	33.	DED1033	Disc pad D
	34.	DED1034	Disc pad E

Mark	No.	Part No.	Description
	101.		Bottom panel
	102.		Stop plate
	103.		Sheet A
	104.		Sheet B
	105.		Reinforce plate
	106.		Rack holder

2. 2 FRONT PANEL SECTION



2. 3 EXTERIOR SECTION (2)



See Fig. 2-2

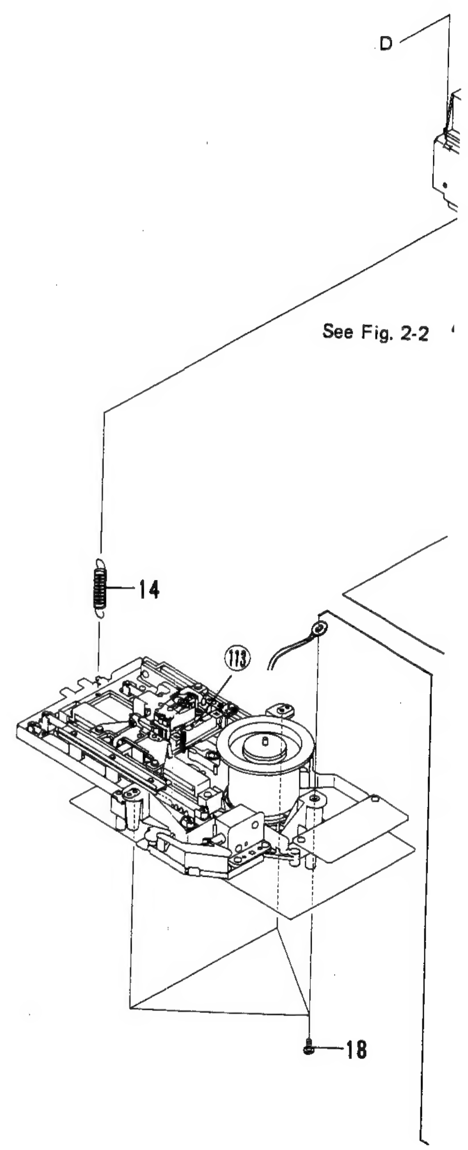
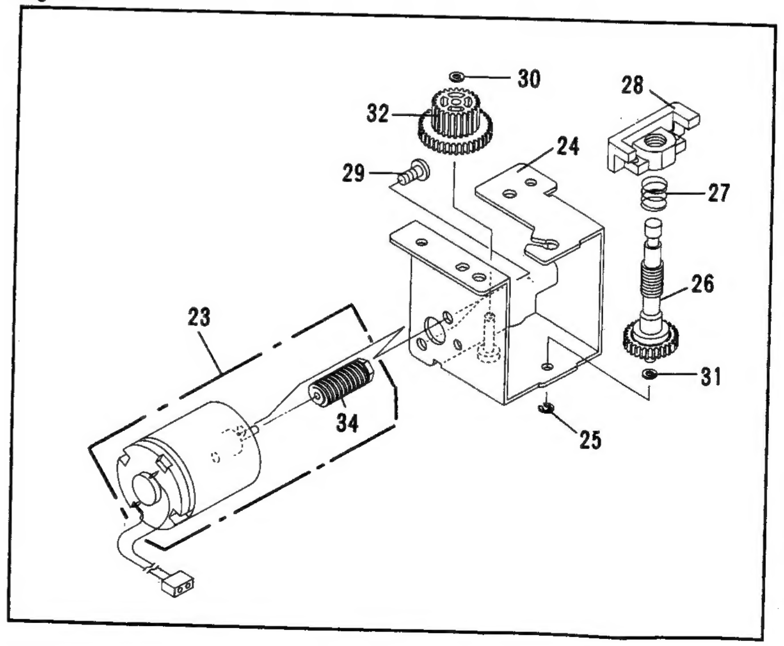


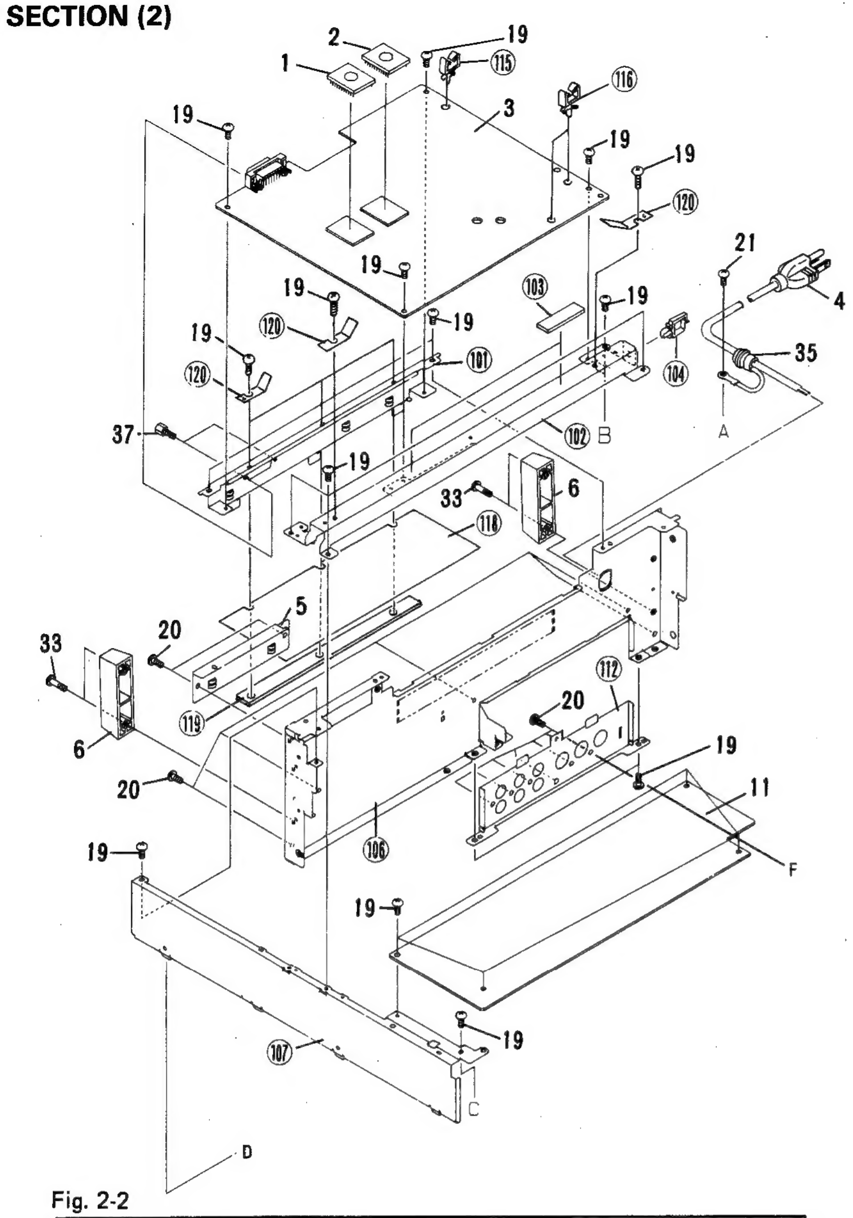
Fig. 2-2



• **Parts List of Front Panel Assembly Section**

Mark	No.	Part No.	Description
	1.	DXX1220	Front panel assembly-S
	2.	DNH1256	GND plate
	3.	VCX-006	Hour meter
	4.	DNK1328	Control button
	5.	DNK1329	Power button
	6.	DBH1043	Power button spring
	7.	BPZ30P080FMC	Screw
	8.	BBZ30P080FMC	Screw
	101.		HOUR assembly
	102.		JACK assembly
	103.		KEYB assembly
	104.		Mine jack holder
	105.		PWID assembly
	106.		Sheet B
	107.		Sheet A
	108.		Front panel assembly

2. 3 EXTERIOR SECTION (2)



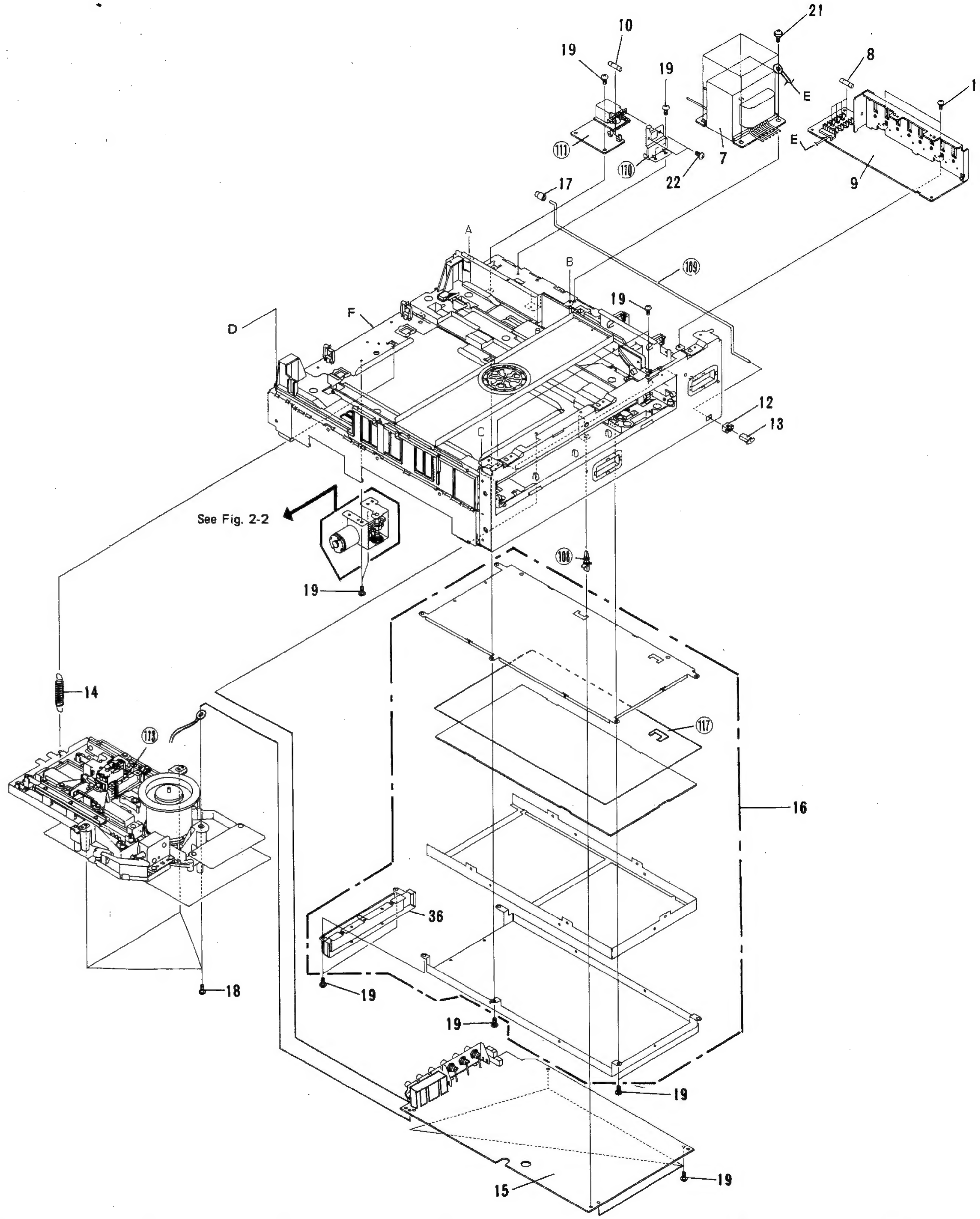
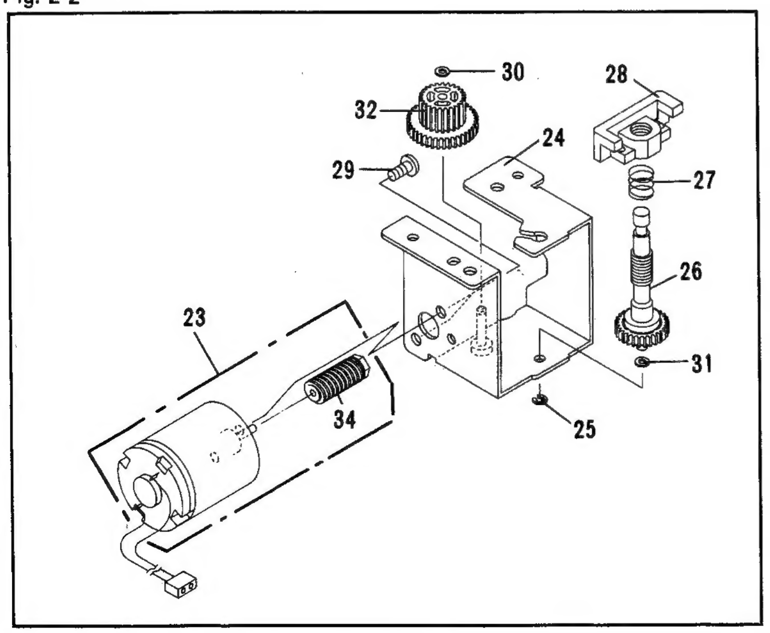


Fig. 2-2



A

B

C

D

y

er

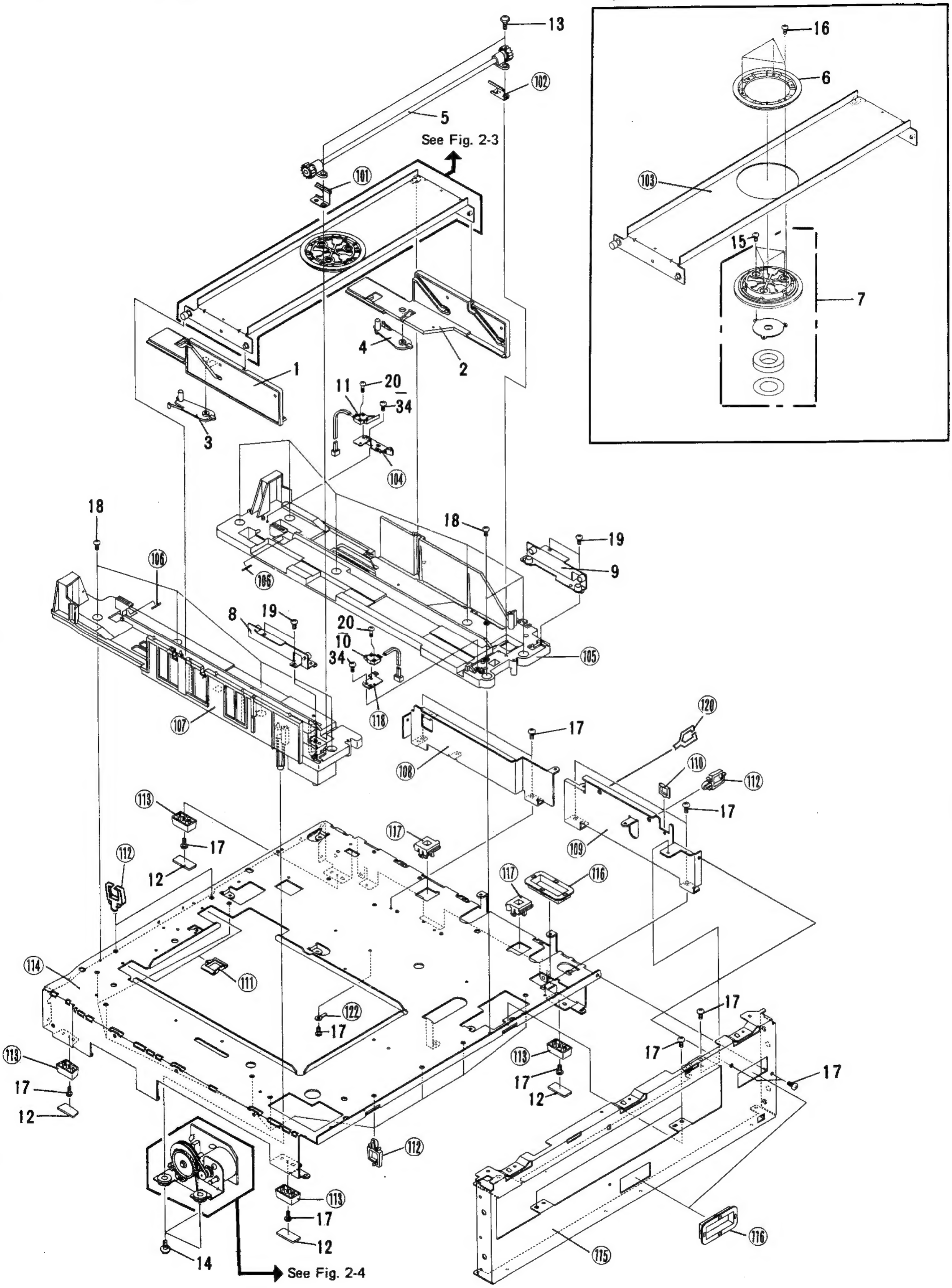
embly

Parts List of Exterior Section (2)

Mark	No.	Part No.	Description
	1.	DYW1041	Program EP-ROM (IC9)
	2.	DYW1042	Program EP-ROM (IC10)
	3.	DWG1076	DSCO assembly
	4.	DDG1001	AC power cord
	5.	DNC1071	Sub rear panel (C)
	6.	VNL-181	Protector
⚠	7.	DTT1027	Power transformer (T1)
⚠	8.	VEK-018	Fuse (FU2 — FU5) (3A)
	9.	DWR1032	REGB assembly
⚠	10.	VEK-021	Fuse (FU1)
	11.	DWV1034	DADB assembly
	12.	DNK1326	PSW bush
	13.	DNK1325	PSW cap
	14.	DBH1048	Tilt spring
	15.	DWV1033	DEGE assembly
	16.	DWV1035	DTMC assembly
	17.	DEB1057	Joint cap
	18.	PMZ30P080FMC	Screw
	19.	BBZ30P080FMC	Screw
	20.	BBT30P080FZK	Screw
	21.	PMZ40P080FMC	Screw
	22.	PMZ30P060FMC	Screw
	23.	DXX1219	Tilt motor assembly-S
	24.	DXB1114	Tilt gear base assembly
	25.	YE20FUC	E-ring
	26.	DXB1118	Tilt shaft assembly
	27.	DBH1051	Limit spring
	28.	DNS1050	Tilt screw
	29.	PMB30P050FMC	Screw
	30.	WT21D040D050	Washer
	31.	WA31D050D050	Washer
	32.	DNK1334	Transmit gear
	33.	VCZ30P200FZK	Screw
	34.	DNK1336	Tilt worm
	35.	VEC-201	Strain relief
	36.	DXX1248	Thru type capacitors assembly
	37.	BBZ30P080FZK	Screw

Mark	No.	Part No.	Description
	101.		Sub rear panel (A)
	102.		Reinforce bridge
	103.		Dumper rubber
	104.		Wire clip
	105.		. . .
	106.		Rear panel
	107.		Reinforce plate
	108.		PC support
	109.		PSW joint
	110.		SW holder
	111.		LSFB assembly
	112.		Sub rear panel (B)
	113.		Mechanism assembly
	114.		Connection bolt
	115.		Wire clip
	116.		Wire clip
	117.		Protect sheet
	118.		Shield sheet
	119.		Shield plate
	120.		Earth rag

2. 4 BASE SECTION

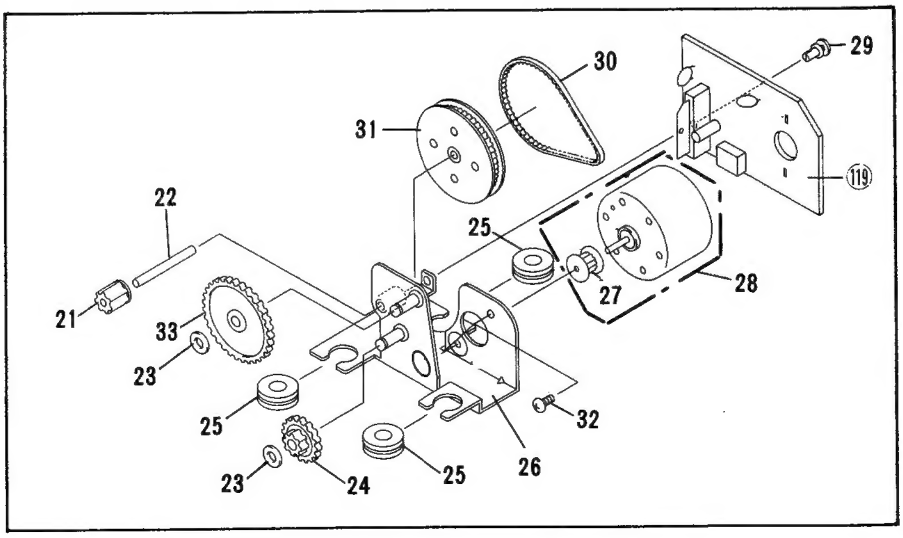


• Parts List of Base Section

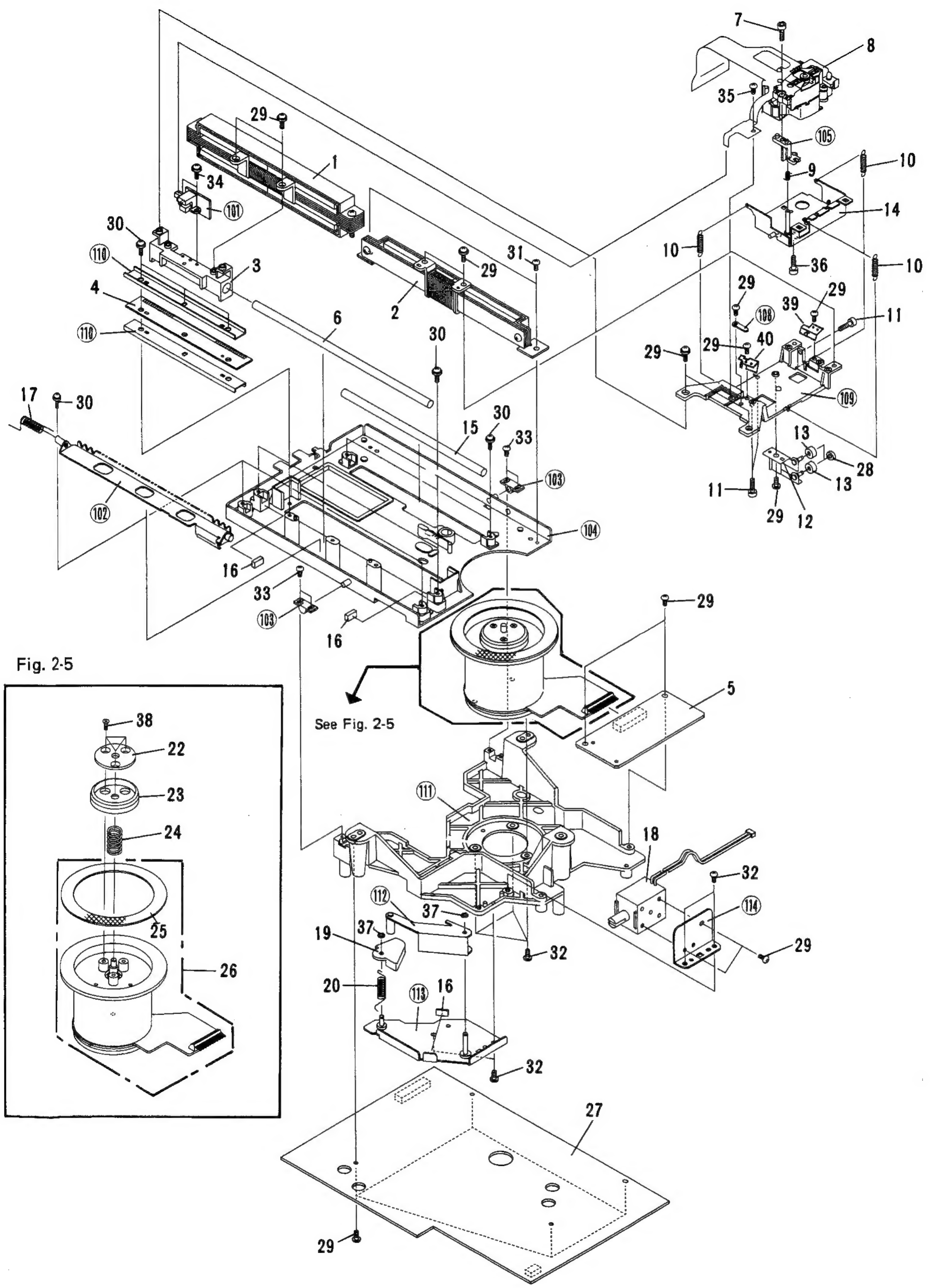
Mark	No.	Part No.	Description
	1.	VNL1068	Clamp cam (L)
	2.	VNL1069	Clamp cam (R)
	3.	VNL1070	Lock lever (L)
	4.	VNL1071	Lock lever (R)
	5.	DXB1109	Synchronized gear assembly
	6.	VNL1130	Clamper head
	7.	VXX1157	Disc clamper assembly-S
	8.	DXB1106	Roller plate (L) assembly
	9.	VXA1162	Roller plate (R) assembly
	10.	VSK-012	Slide switch (TABLE/OUT) (S3)
	11.	VSK-010	Slide switch (TABLE/IN) (S2)
	12.	DEB1066	Leg pad
	13.	VBA1002	Screw
	14.	VBA1003	Screw
	15.	CMZ20P050FMC	Screw
	16.	BPZ26P060FCU	Screw
	17.	BBZ30P080FMC	Screw
	18.	ABZ30P080FMC	Screw
	19.	BPZ30P080FCU	Screw
	20.	BMZ20P080FCU	Screw
	21.	VNL1020	Gear (A)
	22.	VLL1037	Gear (A) shaft
	23.	WT32D060D050	Washer
	24.	VNL1010	Gear (C)
	25.	VEB1025	Rubber bushing
	26.	VXA1088	Motor base assembly
	27.	VNL1051	Motor pulley
	28.	VXX1084	Loading motor assembly-S
	29.	VEC-143	Plastic rivet
	30.	VEB-125	Synchronized belt L
	31.	VXA-477	Pulley (L) assembly
	32.	PMB26P040FMC	Screw
	33.	VNL1064	Gear (B)
	34.	BPZ30P080FMC	Screw
	35.	DNK1341	Rod holder

Mark	No.	Part No.	Description
	101.		Synchronized plate (L)
	102.		Synchronized plate (R)
	103.		Clamper holder assembly
	104.		SW holder (A)
	105.		Plastic base R
	106.		Base clamp rubber
	107.		Plastic base L
	108.		Inner plate (R)
	109.		Inner plate (F)
	110.		Edge guard
	111.		Edge guard
	112.		Wire clip
	113.		Reg
	114.		Chassis base
	115.		Front plate
	116.		Protector
	117.		. . .
	118.		SW holder (B)
	119.		LMCB assembly
	120.		Wire clip
	121.		Wire clip
	122.		Cord stopper plate

Fig. 2-4



2. 5 MECHANISM ASSEMBLY

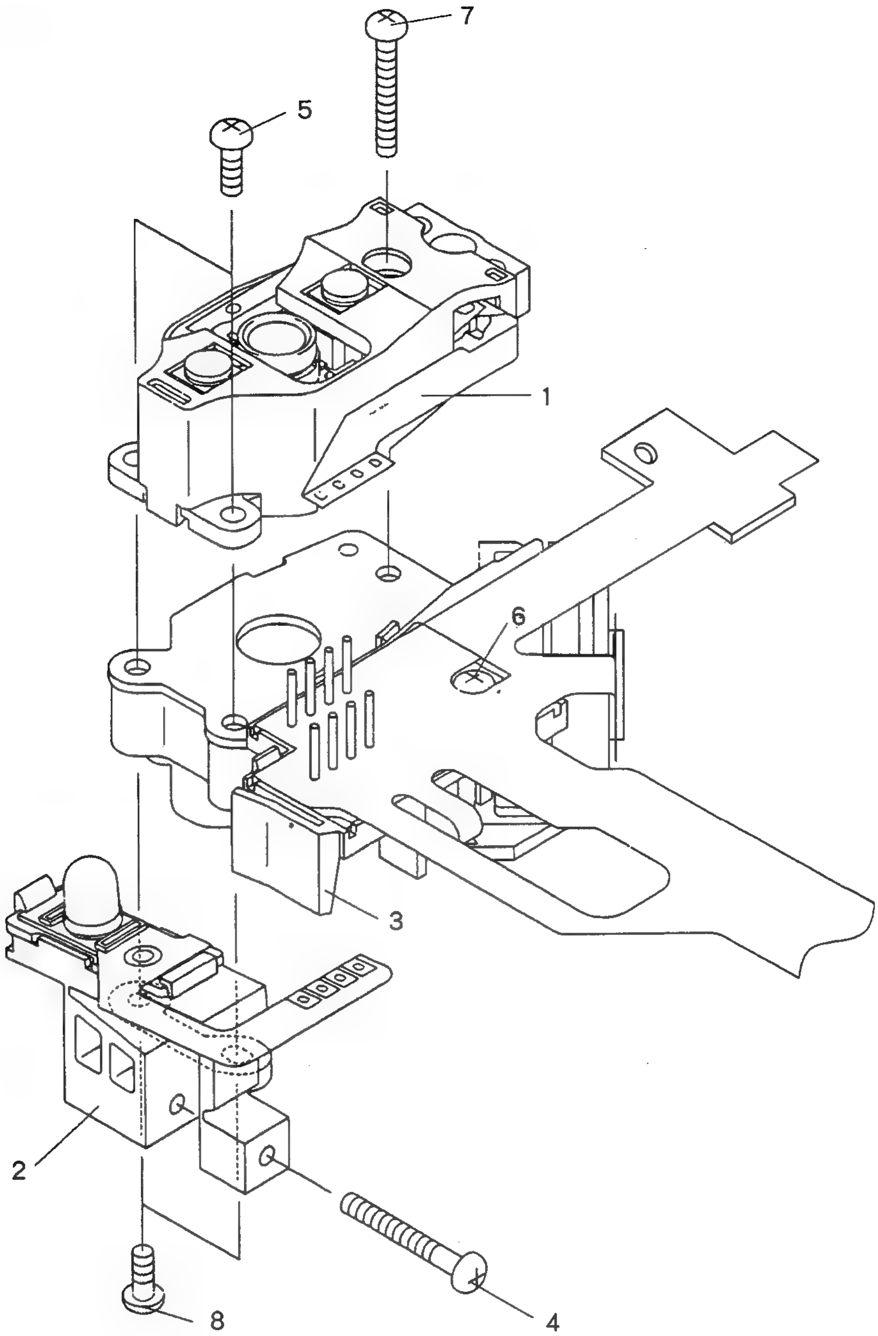


• Parts List of Mechanism Assembly

Mark	No.	Part No.	Description
	1.	DXP1005	Drive unit
	2.	DXP1006	Speed Det. unit
	3.	DNS1051	Shaft catcher
	4.	DNH1166	Slit plate
	5.	DWR1031	BLDB assembly
	6.	DLA1172	D shaft
	7.	VLL1107	Bolt
	8.	DWY1007	Pick-up assembly
	9.	DBH1044	HT spring
	10.	DBH1045	Fixation spring
	11.	DBA1013	Adjustment screw
	12.	DXB1112	Roller plate assembly
	13.	DXB1121	Bearings
	14.	DXB1111	Adjustment plate assembly
	15.	DLA1173	S shaft
	16.	DEB1053	Stopper
	17.	DBH1046	Lock spring
	18.	DXP1001	Plunger
	19.	DNK1333	Lock cam
	20.	DBH1047	Cam spring
	21.	. . .	. . .
	22.	VNE1103	Plate
	23.	DLA1152	Centering hab
	24.	DBH1049	Centering spring
	25.	DEB1052	Rubber spacer
	26.	DXX1246	Spindle motor assembly-S
	27.	DWV1032	PREB assembly
	28.	WT26D047D050	Washer
	29.	PMB30P060FMC	Screw
	30.	IPZ30P080FMC	Screw
	31.	BBZ30P080FMC	Screw
	32.	PMB30P080MC	Screw
	33.	PMH30P120FMC	Screw
	34.	AMZ20P040FMC	Screw
	35.	PMZ26P040FMC	Screw
	36.	SMZ26H120FZK	Screw
	37.	WT26D050D050	Screw
	38.	CBZ30P080FCC	Screw
	39.	DBK1024	G plate (R)
	40.	DBK1023	G plate (L)

Mark	No.	Part No.	Description
	101.		POSS assembly
	102.		Lock teeth assembly
	103.		Optical holder
	104.		Tilt base
	105.		PU holder
	106.		. . .
	107.		. . .
	108.		Cord stopper
	109.		Slider
	110.		Reinforce plate
	111.		Mechanism chassis
	112.		Lock arm assembly
	113.		Lock base assembly
	114.		Plunger base

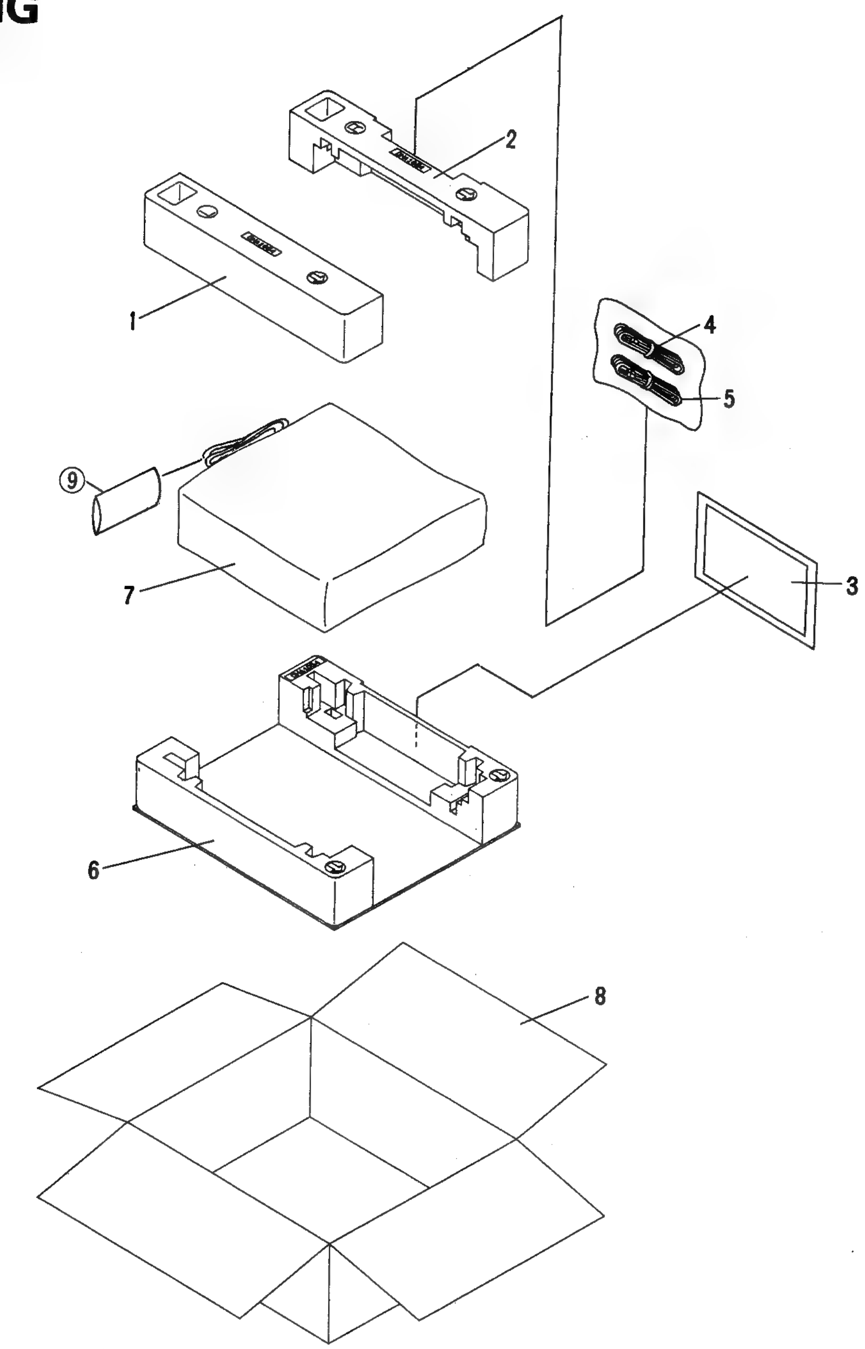
2. 6 PICK-UP ASSEMBLY (DWY1007)



• **Parts List of Pick-up Assembly**

Mark	No.	Part No.	Description
	1.	VXX1241	Actuator assembly
	2.	VXX1094	Sensor assembly-S
	3.	DXX1247	Pre pick-up assembly-S
	4.	PBZ20P160FMC	Screw
	5.	PMA20P060FMC	Screw
	6.	PMA20P080FMC	Screw
	7.	PMA20P140FMC	Screw
	8.	PMB20P050FMC	Screw

3. PACKING



• Parts List of Packing

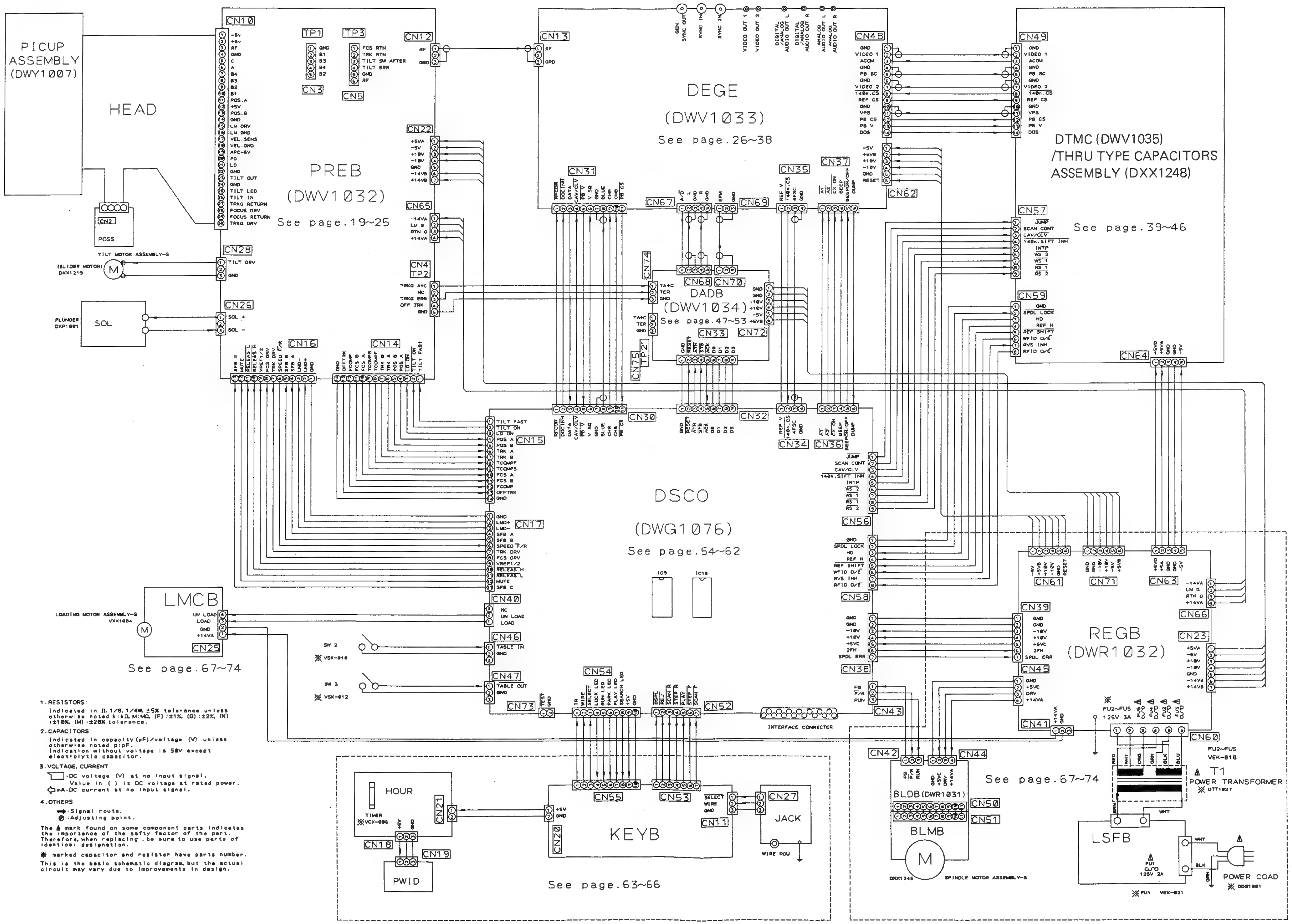
Mark	No.	Part No.	Description
	1.	DHA1054	Top pad L
	2.	DHA1055	Top pad R
	3.	DRB1013	Operating instructions
	4.	VDE-014	Video cable
	5.	VDE-055	Connection cord
	6.	DHA1056	Bottom pad
	7.	VHL1005	Packing mat
	8.	DHG1096	Packing case
	9.		Polyethylene bag

• Notes of P.C. Board Patterns

P.C.B. pattern diagram indication	Corresponding part symbol	Part name	P.C.B. pattern diagram indication	Corresponding part symbol	Part name
	E or E	Transistor			Ceramic capacitor
D S G	D S G or D S G	FET			Mylar capacitor
		Diode	SA		Styrol capacitor
			NP		Electrolytic capacitor (Non polarized)
			NL		Electrolytic capacitor (Noiseless)
		Zenner diode		+	Electrolytic capacitor (Polarized)
					Electrolytic capacitor (Polarized)
		LED			Power capacitor
		Varactor			Semi-fixed resistor
		Tact switch			Resistor array
		Inductor			Resistor
		Coil			Resonator
4 3 2 1 5		Transformer			Thermistor
8 1		Filter			

1. This P.C.B. connection diagram is viewed from the parts mounted side.
2. The parts which have been mounted on the board can be replaced with those shown with the corresponding wiring symbols listed in the above Table.
3. The capacitor terminal marked with ▭ shows negative terminal.
4. The diode marked with O shows cathode side.
5. The transistor terminal marked with ▭ shows emitter.

4. CONNECTION DIAGRAM



1. RESISTORS:
Indicated in Ω, 1/8, 1/4W, ±5% tolerance unless otherwise noted k:kΩ, M:MΩ, (F):±1%, (G):±2%, (K):±10%, (M):±20% tolerance.

2. CAPACITORS:
Indicated in capacity (μF)/voltage (V) unless otherwise noted p:pF.
Indication without voltage is 50V except electrolytic capacitor.

3. VOLTAGE, CURRENT
:DC voltage (V) at no input signal.
Value in ( ) is DC voltage at rated power.
mA:DC current at no input signal.

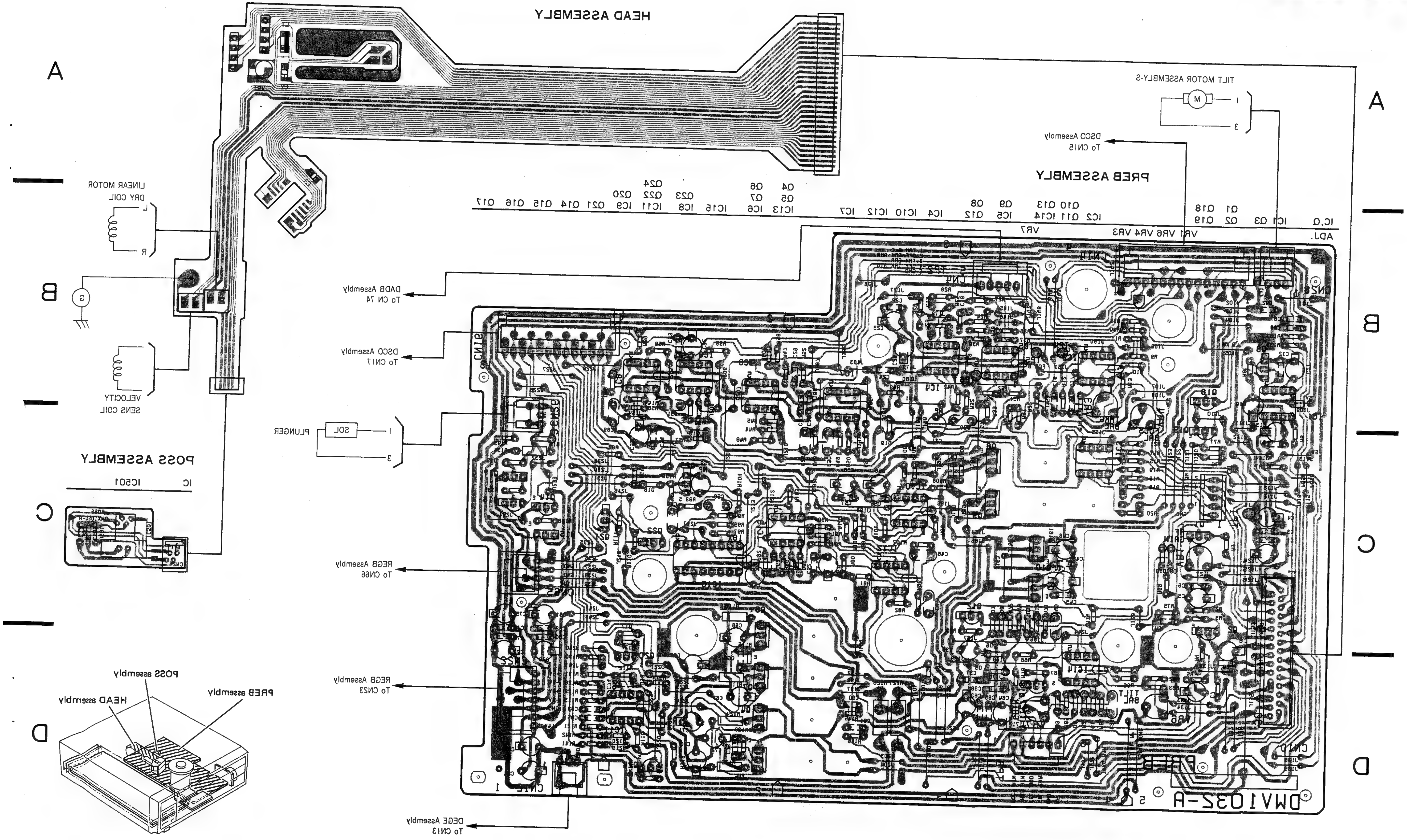
4. OTHERS
:Signal route.
:Adjusting point.

The ⚠ mark found on some component parts indicates the importance of the safty factor of the part. Therefore, when replacing, be sure to use parts of identical designation.

✱ marked capacitor and resistor have parts number.

This is the basic schematic diagram, but the actual circuit may vary due to improvements in design.

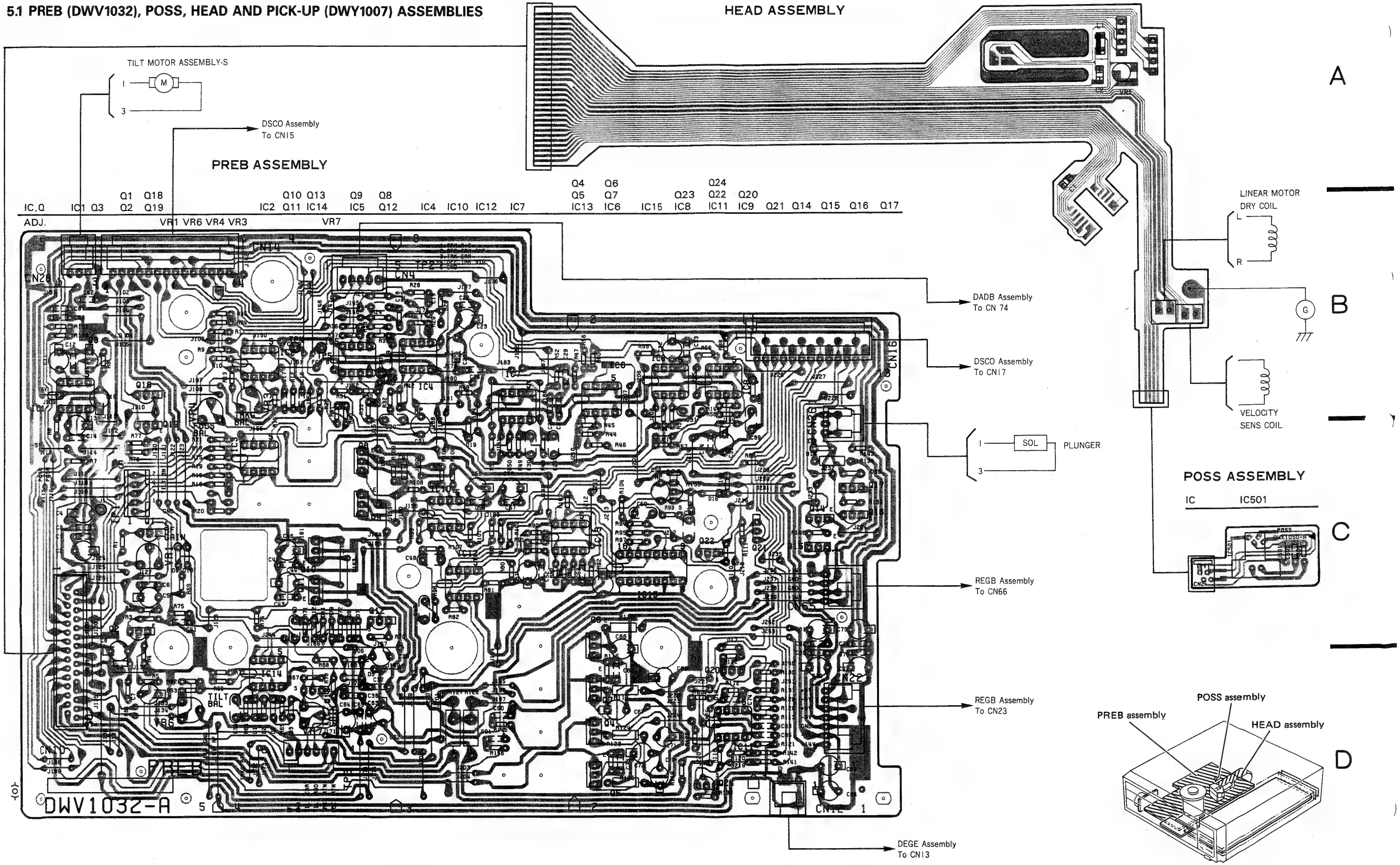
This P.C.B. connection diagram is viewed from the foil side.



5. SCHEMATIC DIAGRAM AND P.C. BOARD PATTERNS

5.1 PREB (DWV1032), POSS, HEAD AND PICK-UP (DWY1007) ASSEMBLIES

This P.C.B. connection diagram is viewed from the parts mounted side.



1 2 3 4

A

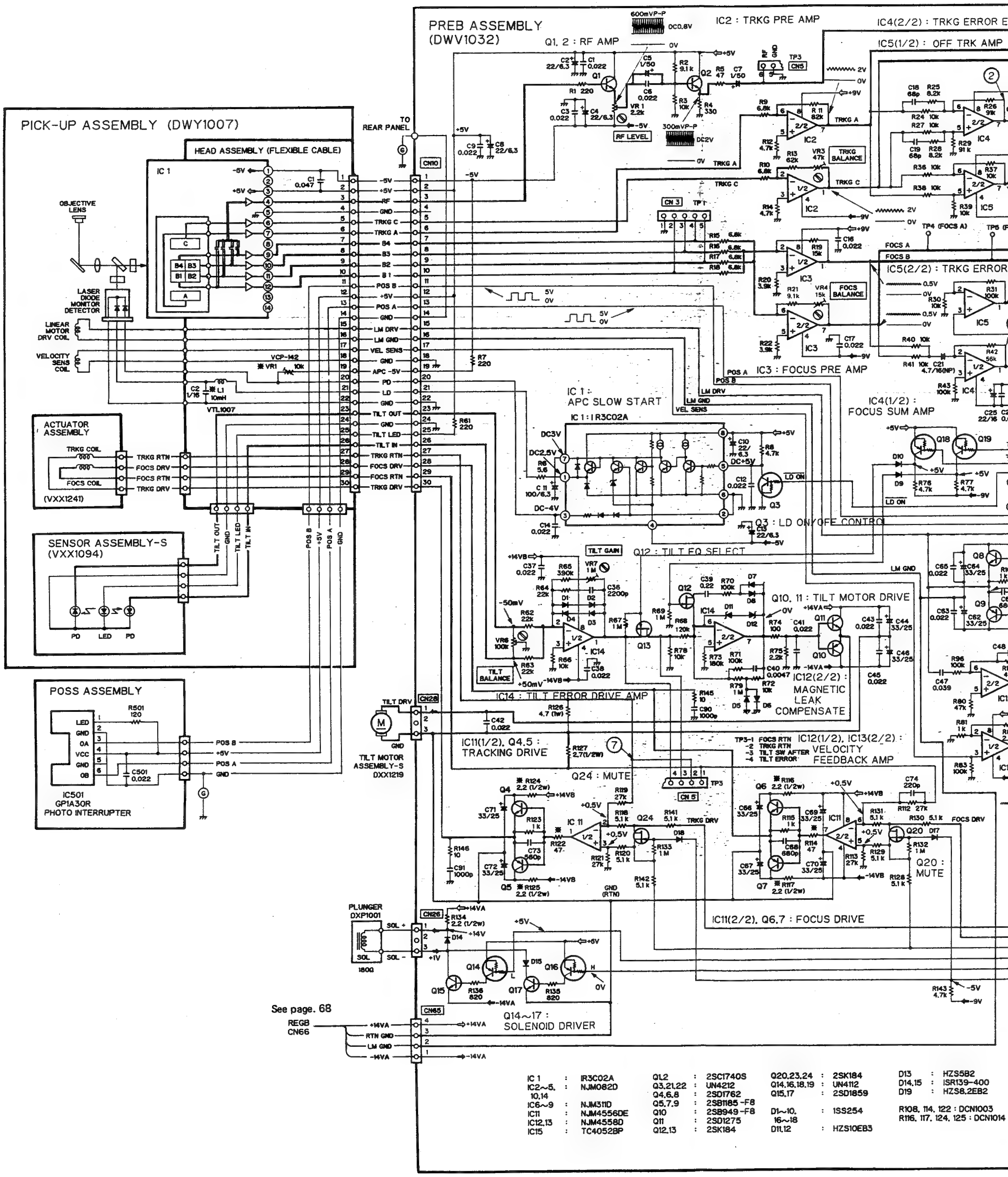
B

C

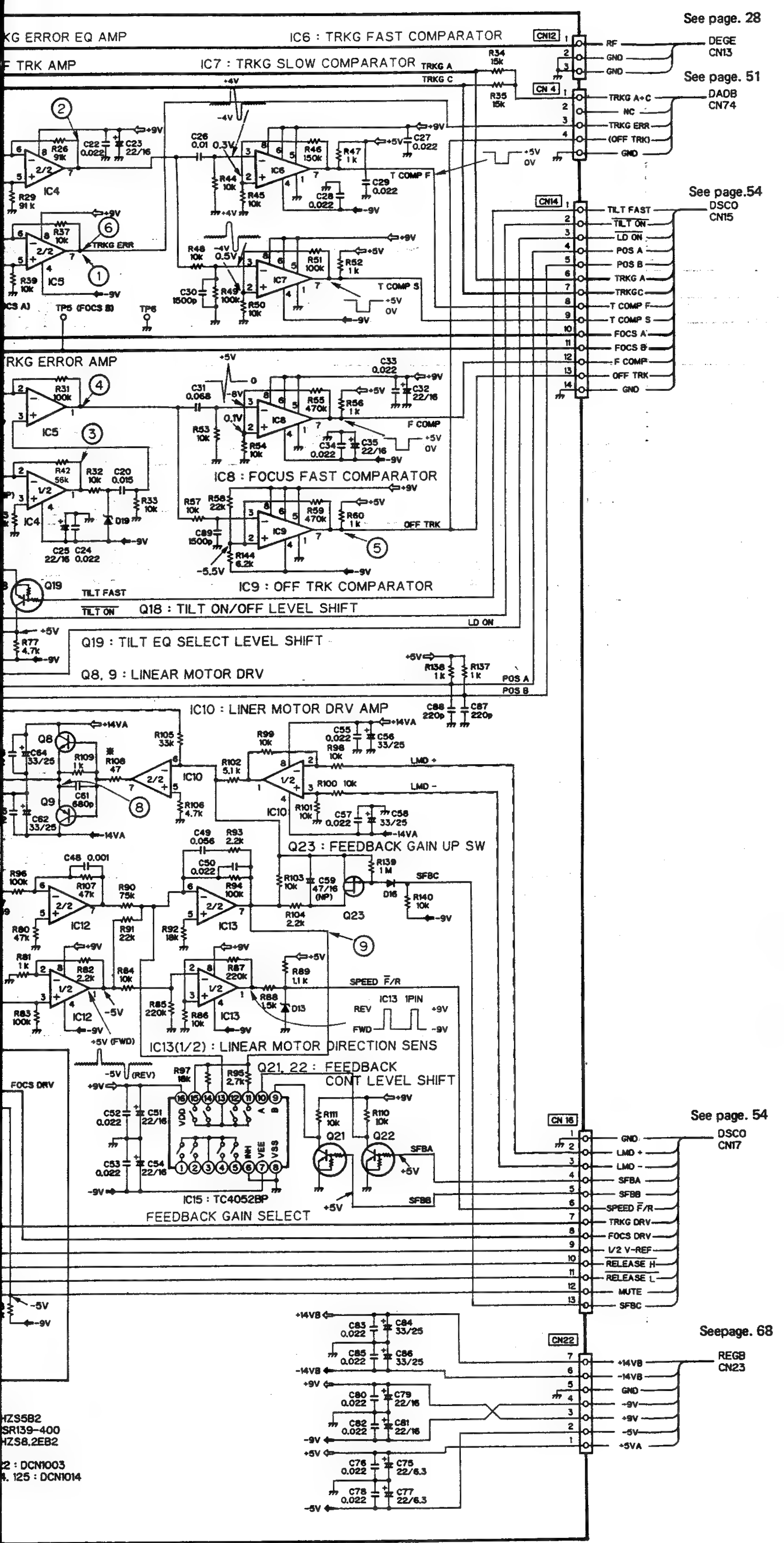
D

E

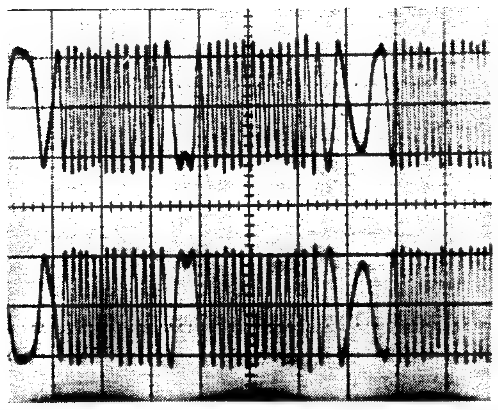
F



1 2 3 4



Wave Forms



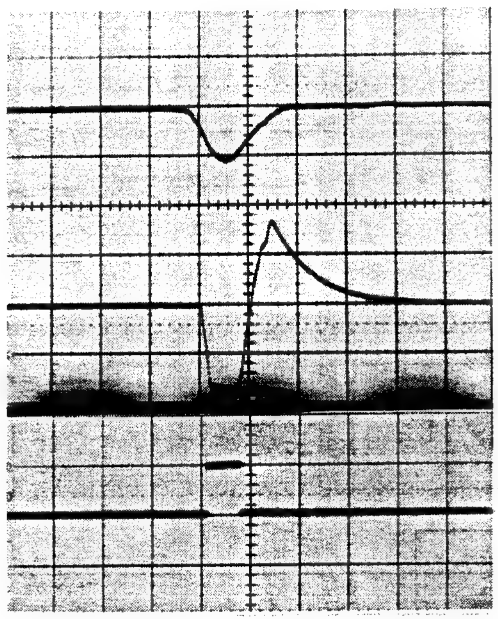
① 0V
② 0V

TRKG OPEN

TP2-3 TRKG ERROR (IC5-Pin7) 0.5V/div

5mS/div

IC4-Pin7 TRKG ERROR EQ AMP OUT 5V/div



③ 0V
④ 0V
⑤ 0V

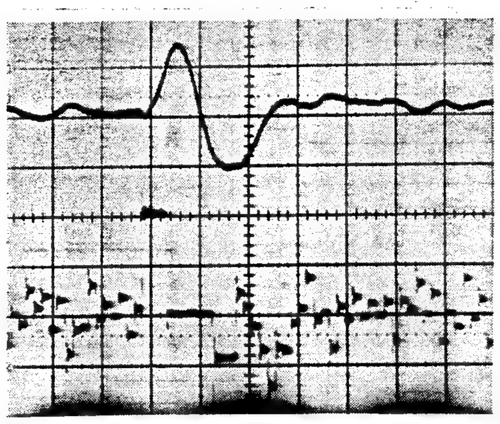
STILL

IC4-Pin1 5V/div

0.2mS/div

IC5-Pin1 5V/div

IC9-Pin7 OFF TRK 5V/div



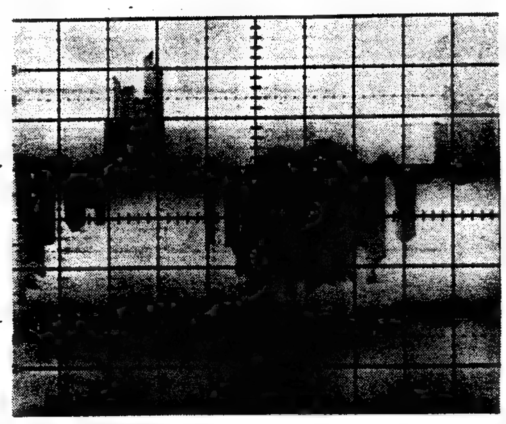
⑥ 0V
⑦ 0V

STILL

TP2-3 TRKG ERROR 1V/div

0.2mS/div

TP3-2 TRKG RTN 0.5V/div



⑧ 0V
⑨ 0V

PLAY, STILL

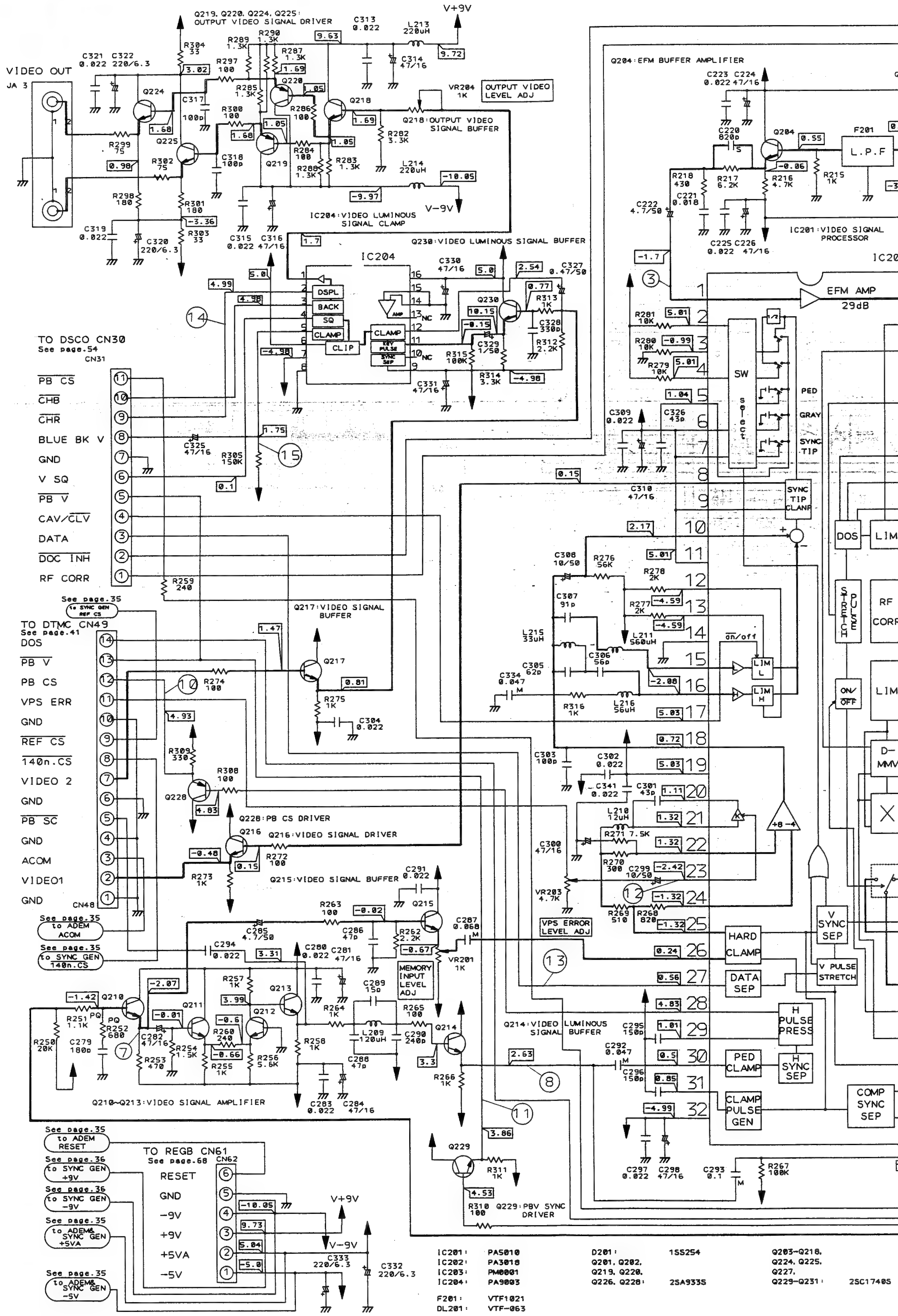
Q8, Q9-E LINEAR MOTOR DRV 5V/div

5mS/div

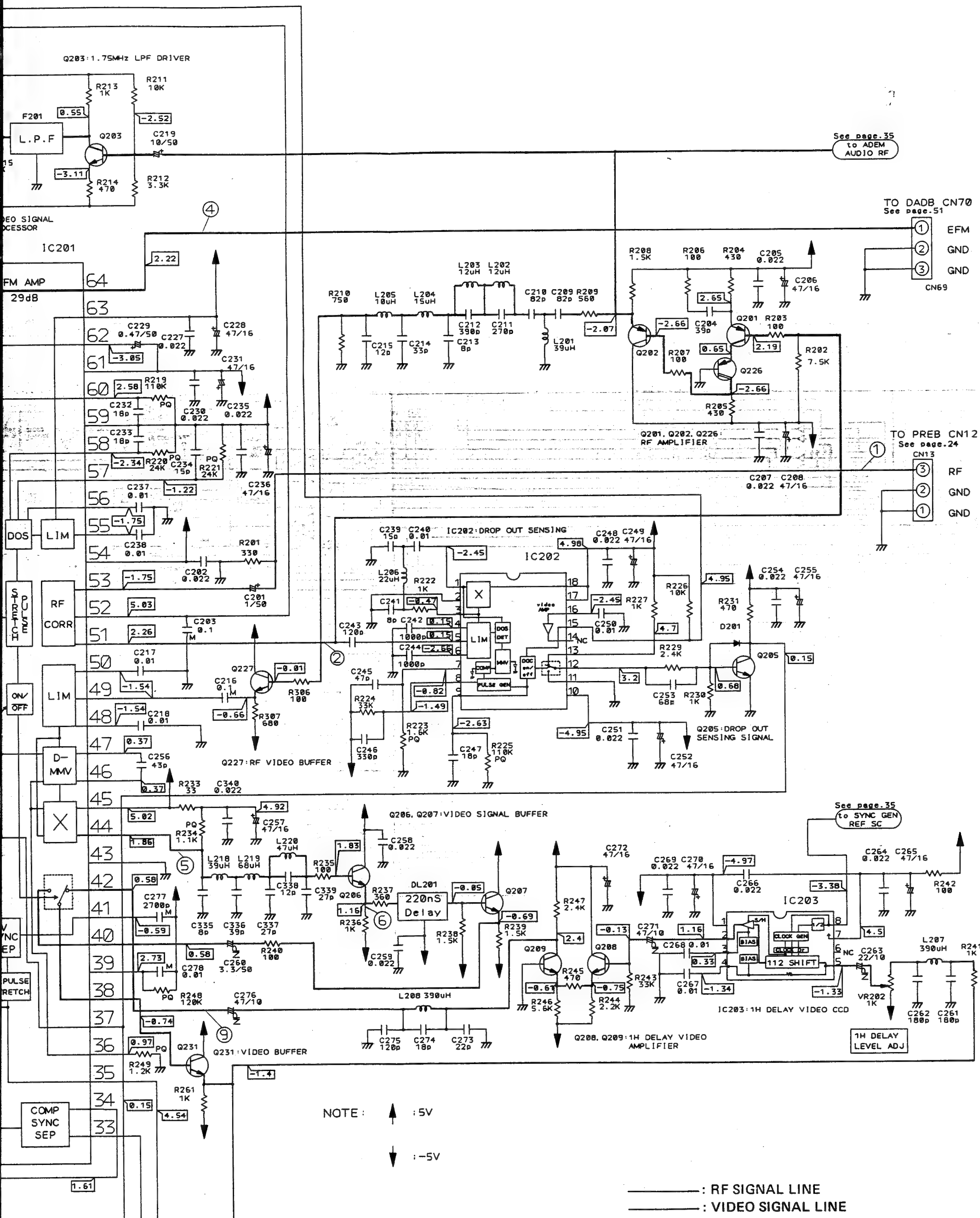
IC13-Pin7 FEED BACK AMP OUT 0.5V/div

———: RF SIGNAL LINE
———: FOCUS SERVO LOOP LINE
———: TILT SERVO LOOP LINE
———: TRACKING SERVO LOOP LINE
- - - - -: LINER MOTOR (SLIDER) SERVO LOOP LINE

5. 2 DEGE (DWV1033) ASSEMBLY (VDEM SECTION)



IC201:	PA5010	D201:	1SS254	Q203-Q218, Q224, Q225, Q227, Q229-Q231:	2SC1740S
IC202:	PA3018	Q201, Q202, Q219, Q220, Q226, Q228:	2SA933S		
IC203:	PM0001				
IC204:	PA9003				
F201:	VTF1021				
DL201:	VTF-063				



NOTE: ↑ :5V

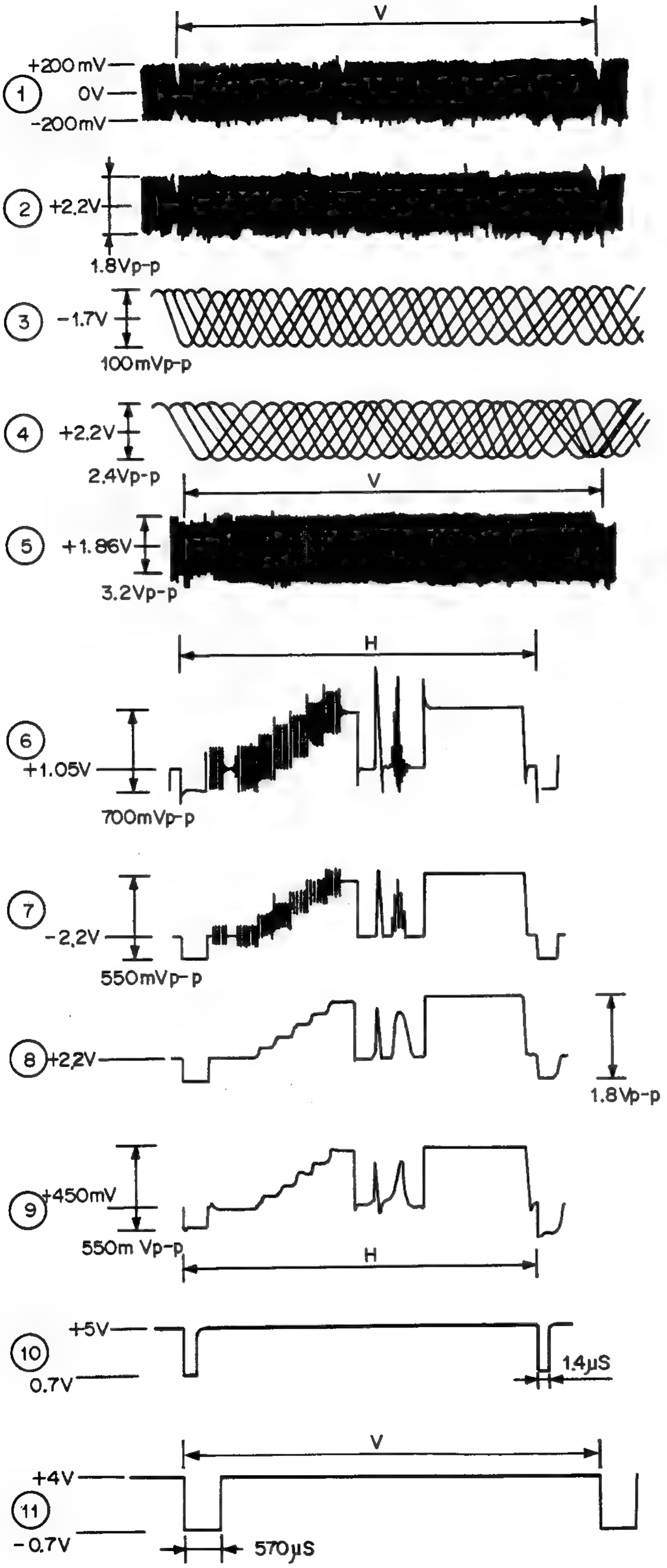
↓ :-5V

: RF SIGNAL LINE

: VIDEO SIGNAL LINE

: EFM SIGNAL LINE

- **Wave Forms**



CN13 3PIN
RF
(F.N.24000. T1)

IC201 51PIN
RF

IC201 1PIN
EFM

IC201 64PIN
EFM

IC201 44 PIN
VIDEO RF

Q206 E

Q210 E
(ALMOST SAME Q216E, Q217E Q218E, Q224E AND Q225E)

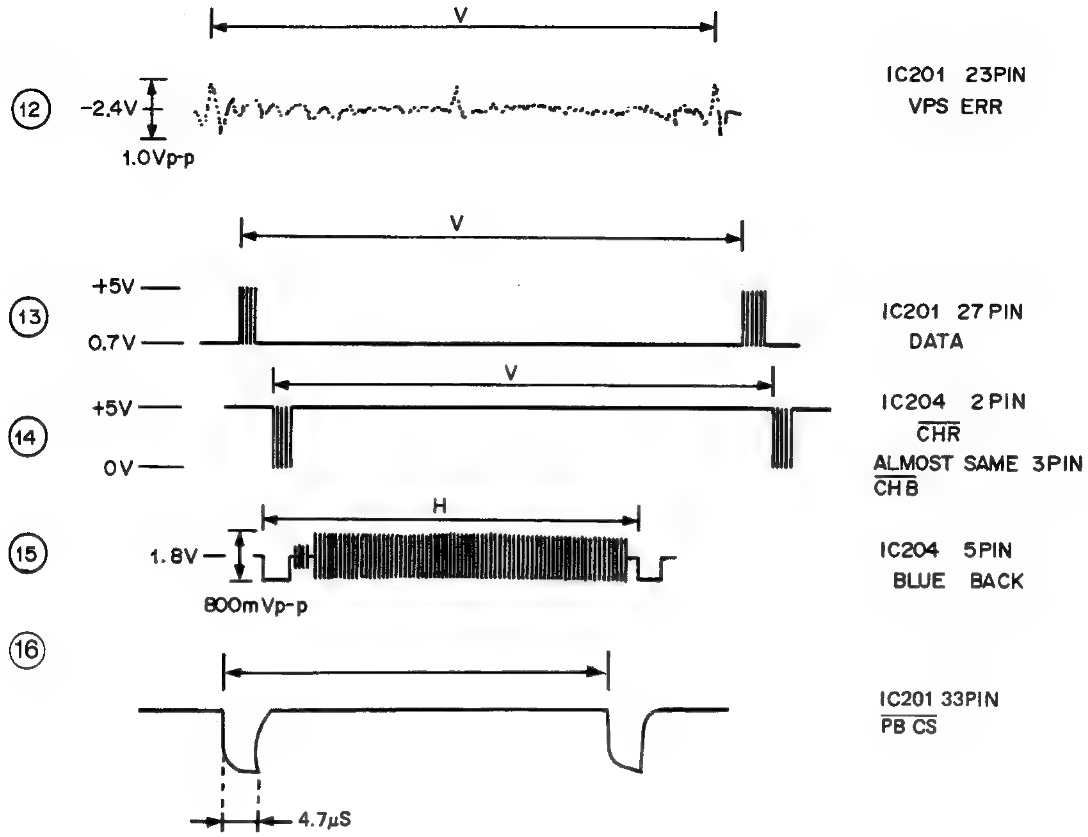
(FOR THE p-p VALUE AND PEDESTAL VOLTAGE THEY HAVE THE DIFFERENT VALUES RESPECTIVELY)
Q214 E

IC201 42PIN
1H DELAY VIDEO

Q228E
PB CS

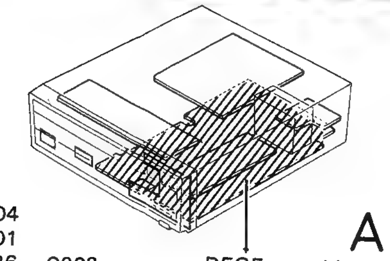
Q229E
PB V

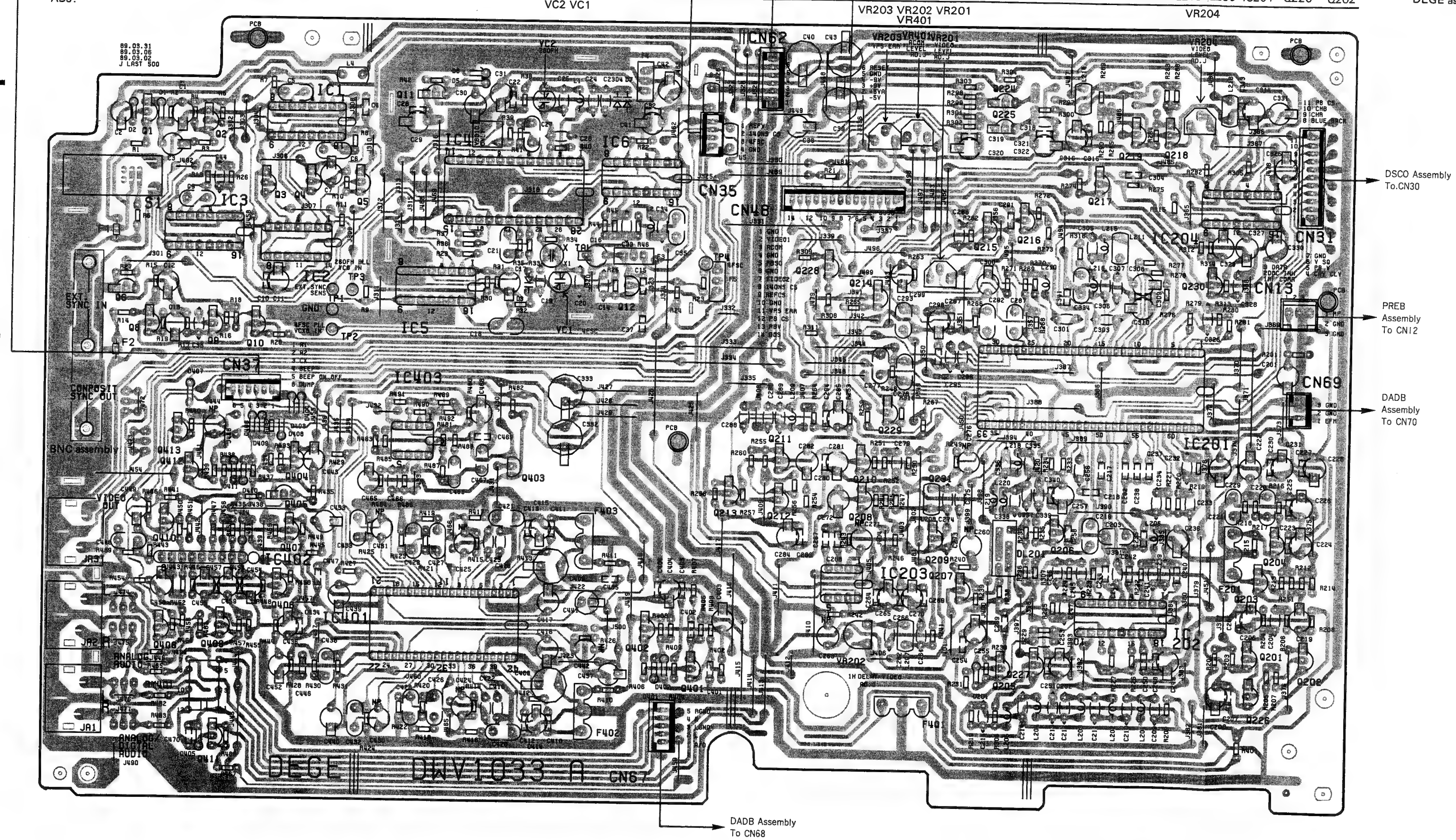
V ⟶ 16.6mS
H ⟶ 63.5µS


V
(12)
-2.4V
1.0Vp-p
IC201 23PIN
VPS ERR
V
(13)
+5V
0.7V
IC201 27 PIN
DATA
V
(14)
+5V
0V
IC204 2 PIN
CHR
ALMOST SAME 3PIN
CHB
H
(15)
1.8V
800mVp-p
IC204 5PIN
BLUE BACK
(16)
IC201 33PIN
PB CS
4.7μS

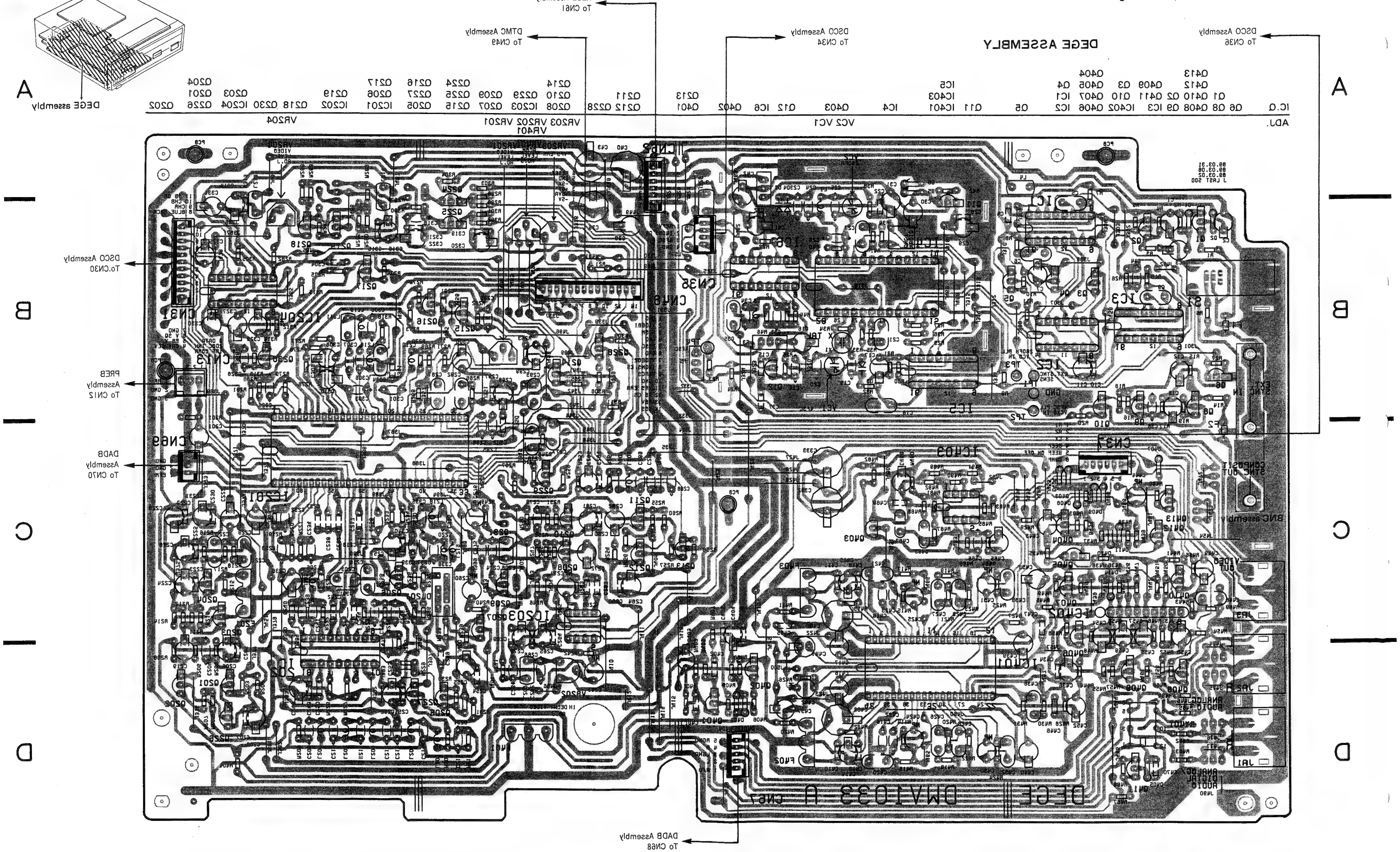
This P.C.B. connection diagram is viewed from the parts mounted side.

DEGE ASSEMBLY

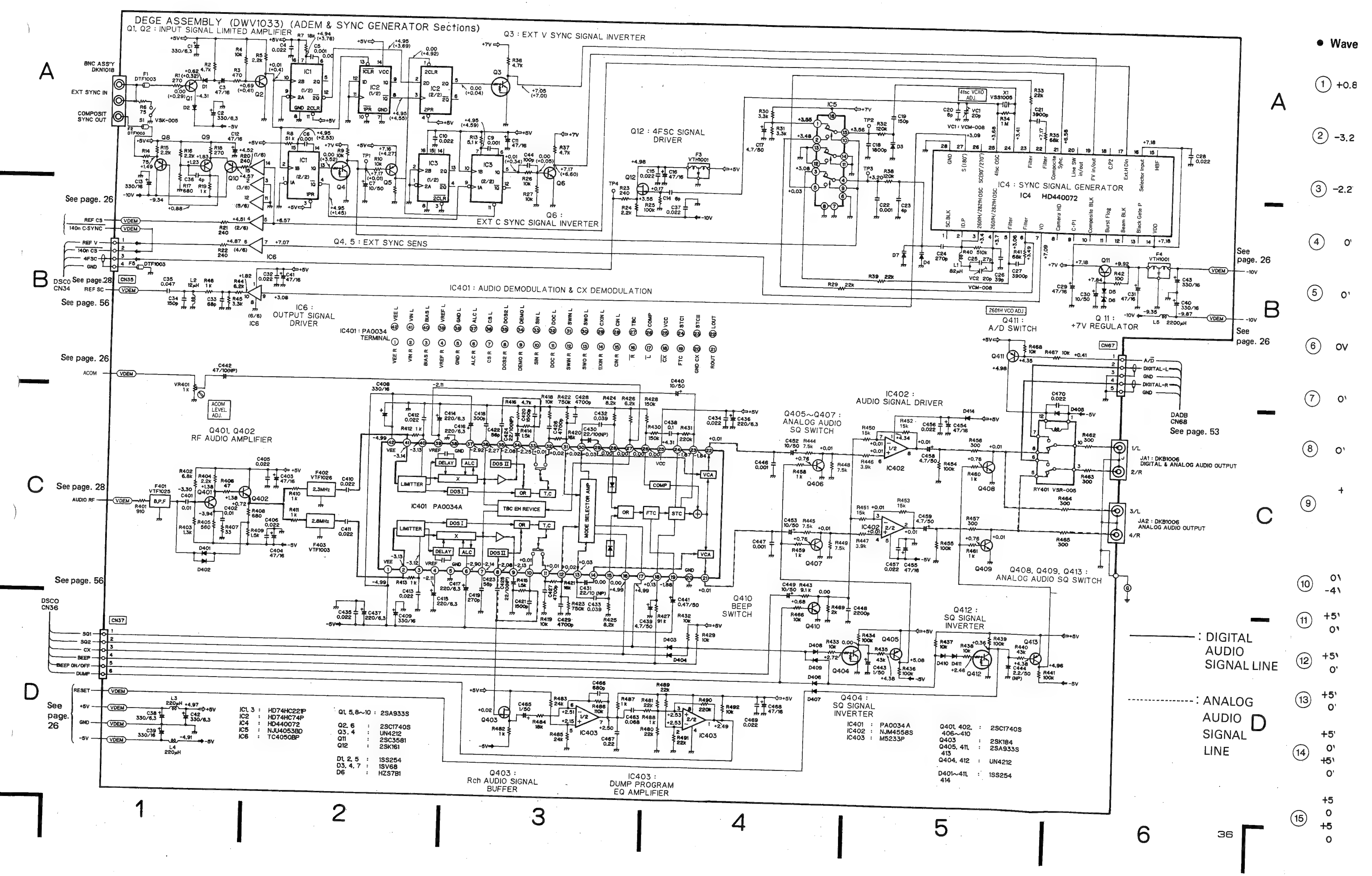




This P.C.B. connection diagram is viewed from the foil side.



5.3 DEGE (DWV1033) ASSEMBLY (ADEM AND SYNC. GENERATOR SECTIONS)



See page. 26

VDEM -10V

VDEM -10V

See page. 26

ige. 53

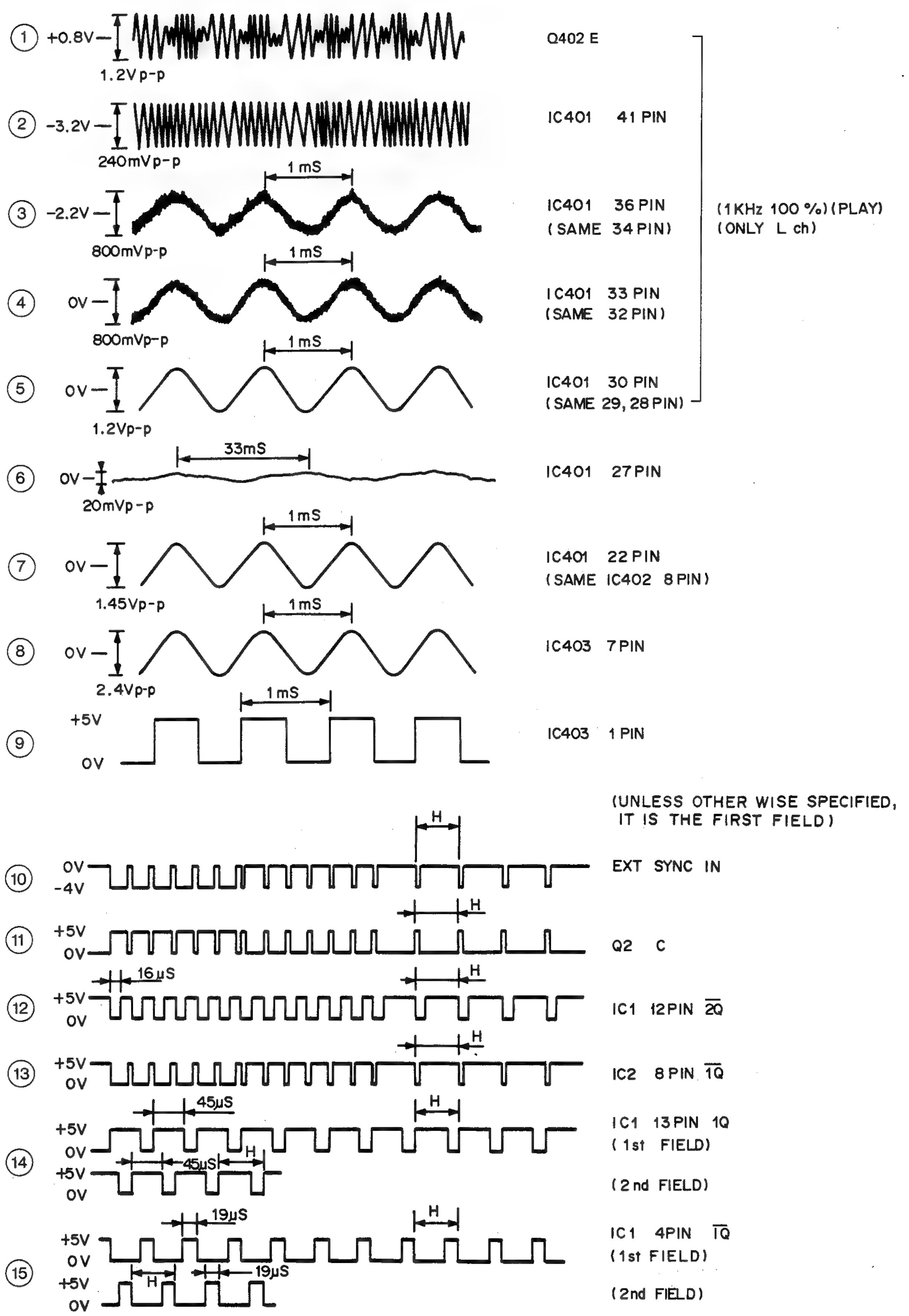
AUDIO OUTPUT

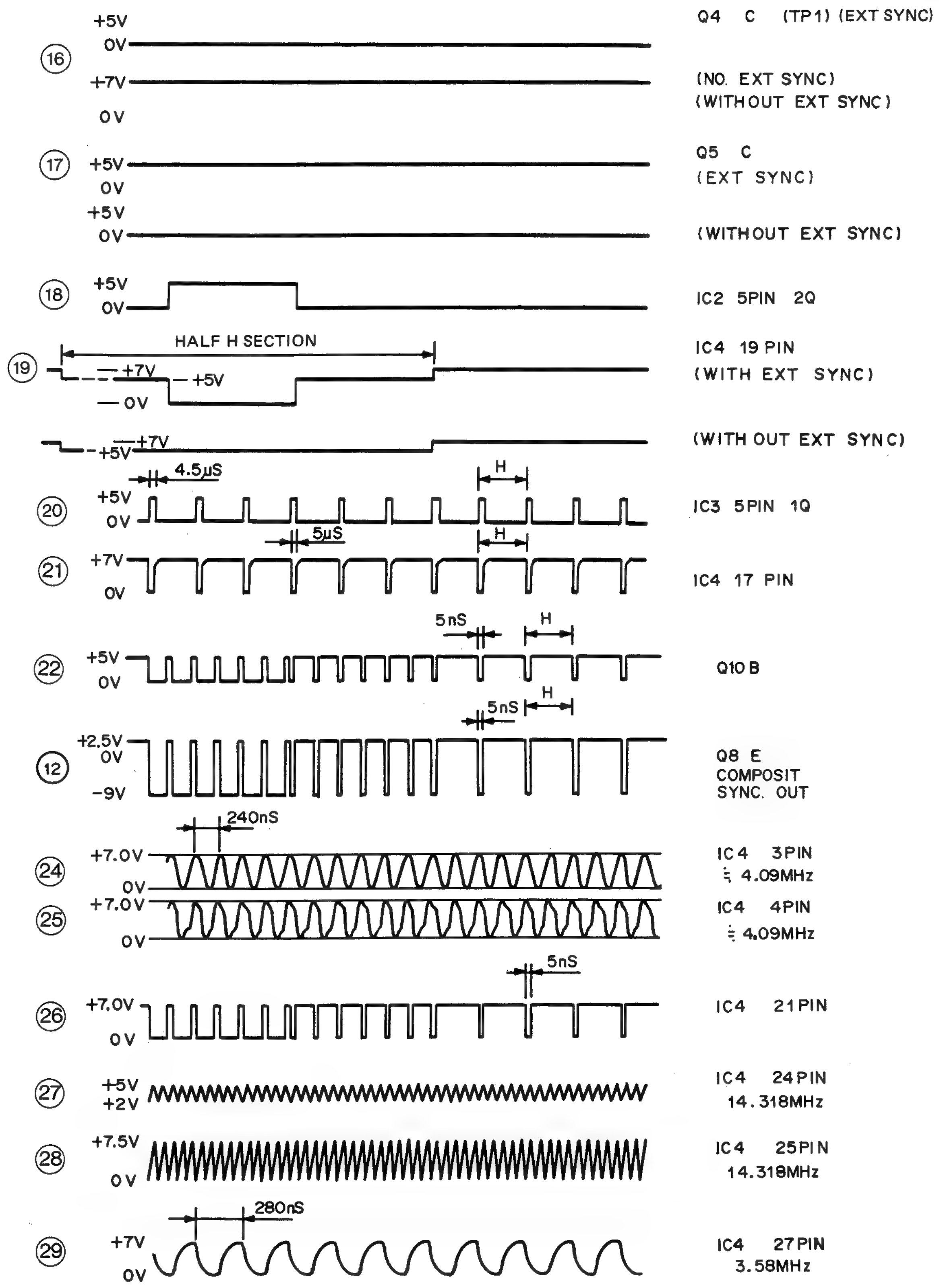
TPUT

-: DIGITAL AUDIO SIGNAL LINE

--: ANALOG AUDIO SIGNAL LINE

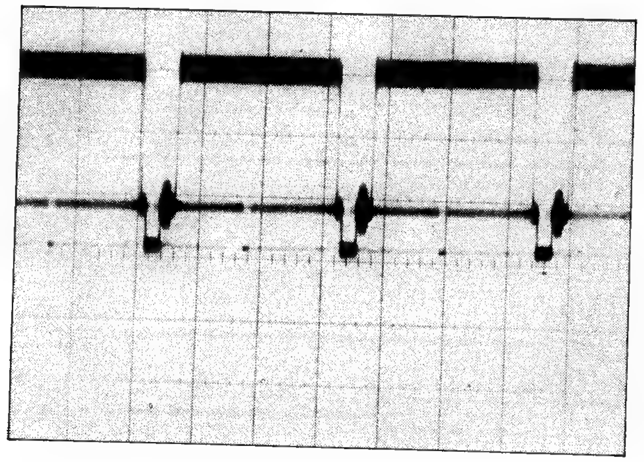
- **Wave Forms**





- **Wave Forms**

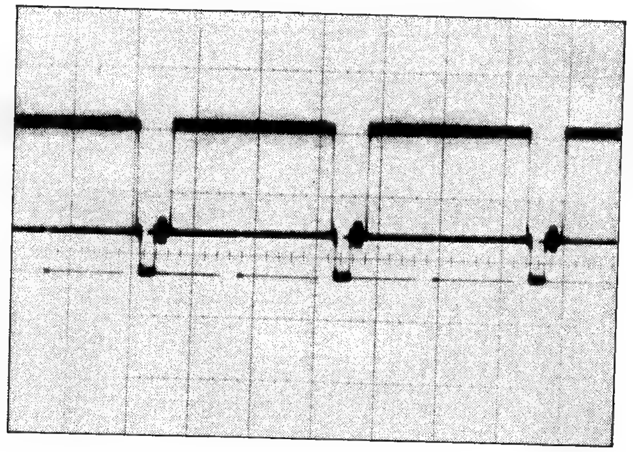
① Q2-B
With white screen



0.5V/div
20μS/div

◄ GND

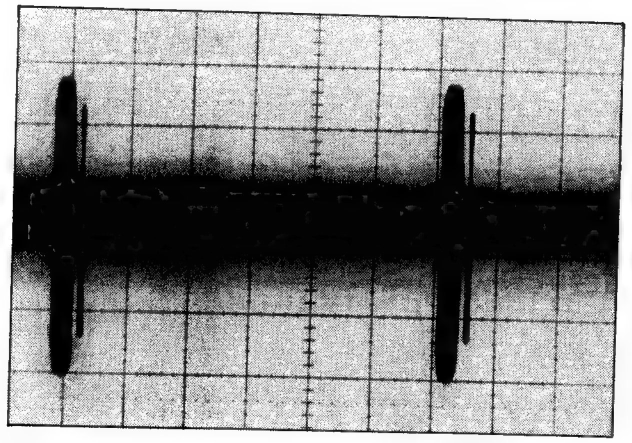
② Q39-E
With white screen



1V/div
20μS/div

◄ GND

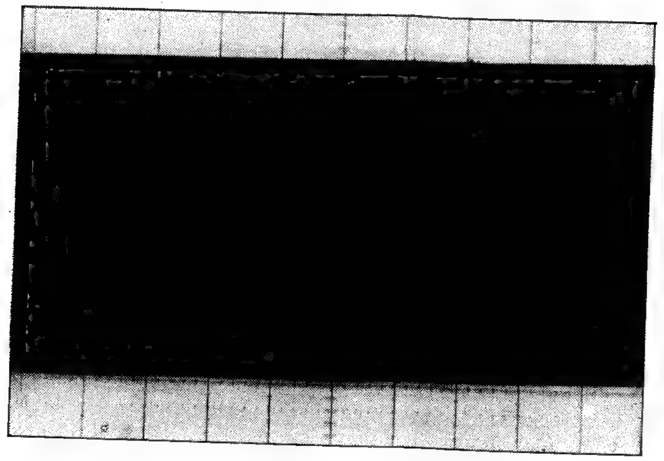
③ IC3-Pin33



1V/div
10μS/div

◄ GND

④ IC14-Pin110
It must be a 4 fsc - continuous waves.



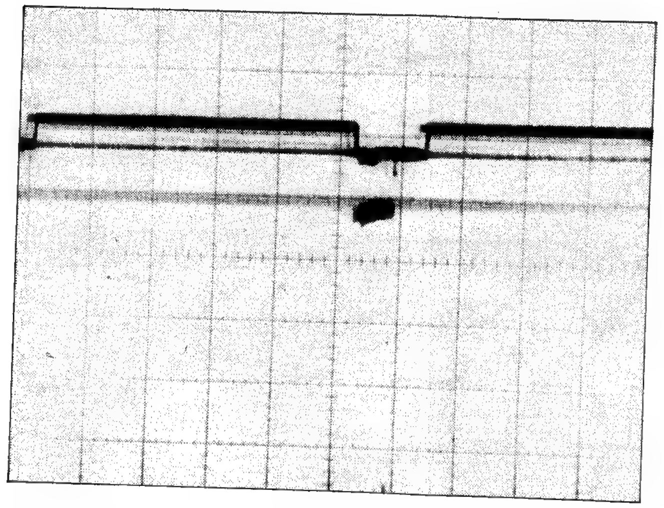
1V/div
1mS/div

◄ GND

⑤ IC15-Pin4
(When playing back white screen)

and timing of IC14-pin 101 waveform

⑥ IC14-Pin101

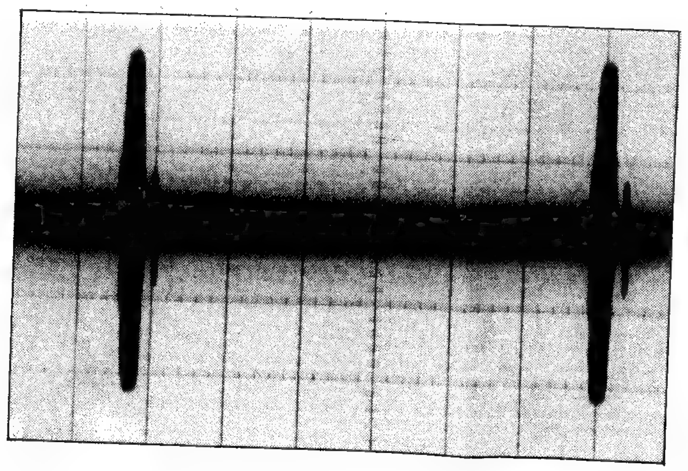


1V/div
10μS/div

◄ Pin4 GND

◄ CBL GND

⑦ IC1-Pin21



0.2V/div
10μS/div

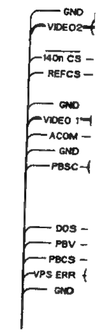
◄ GND

A

B

C

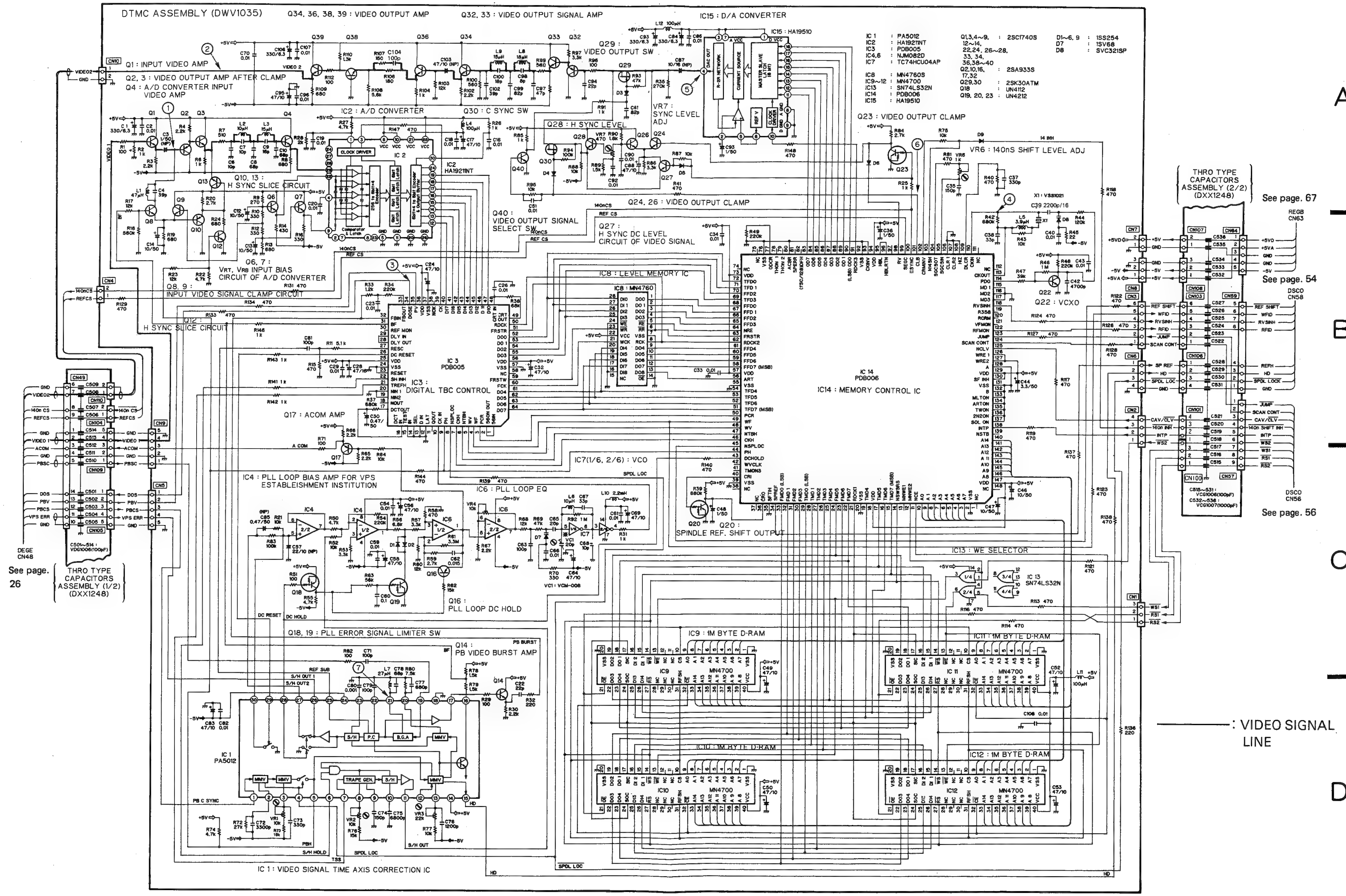
D



DEGE
CN48

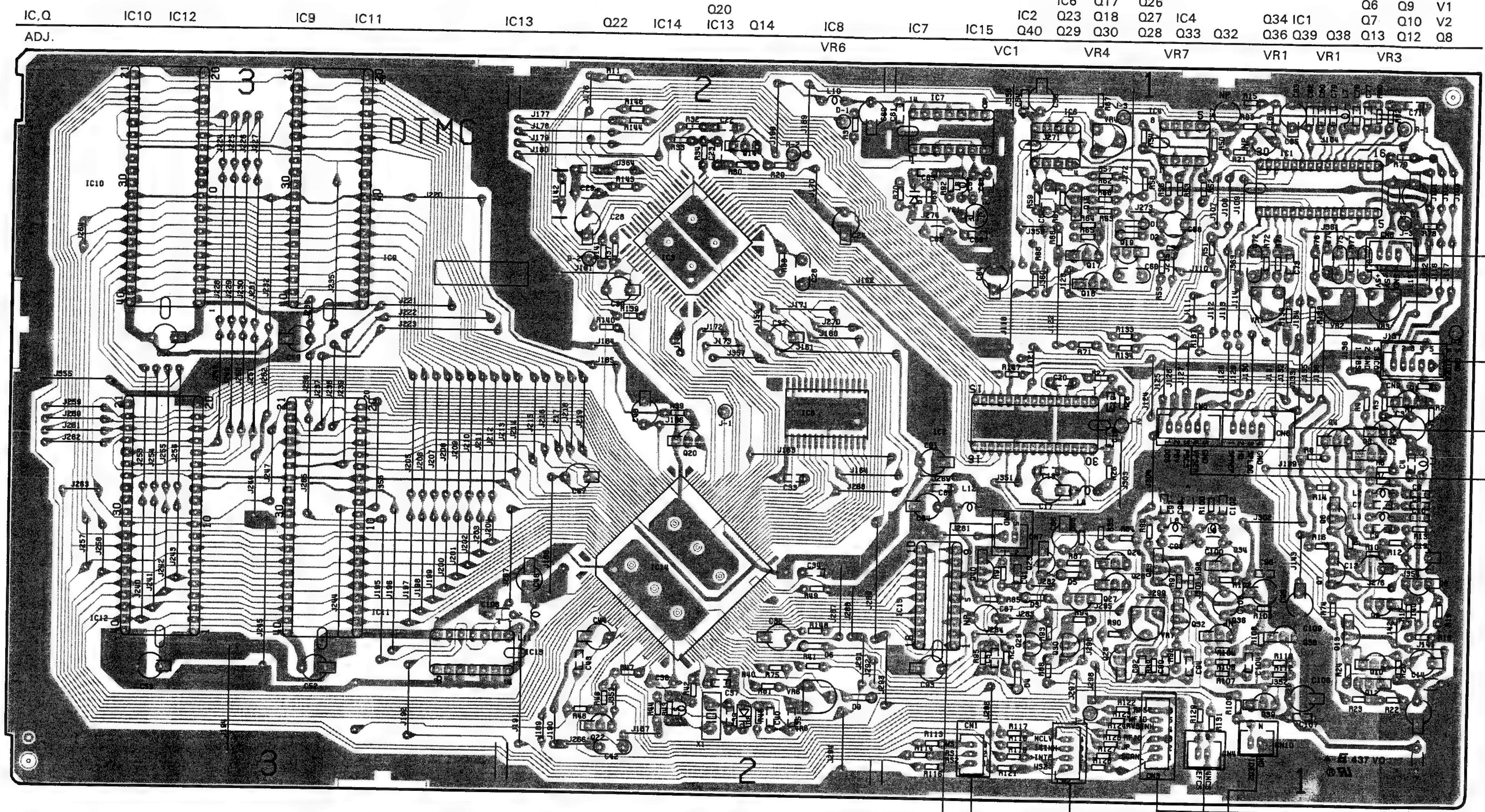
See page. 26

5.4 DTMC (DWV1035) AND THOU TYPE CAPACITORS ASSEMBLIES (DXX1248)

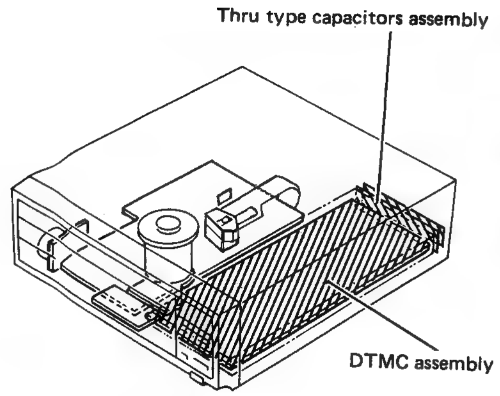


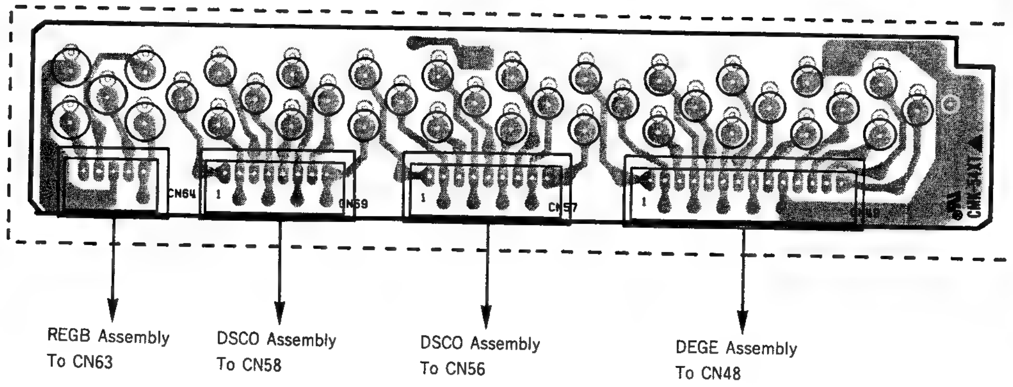
DTMC ASSEMBLY

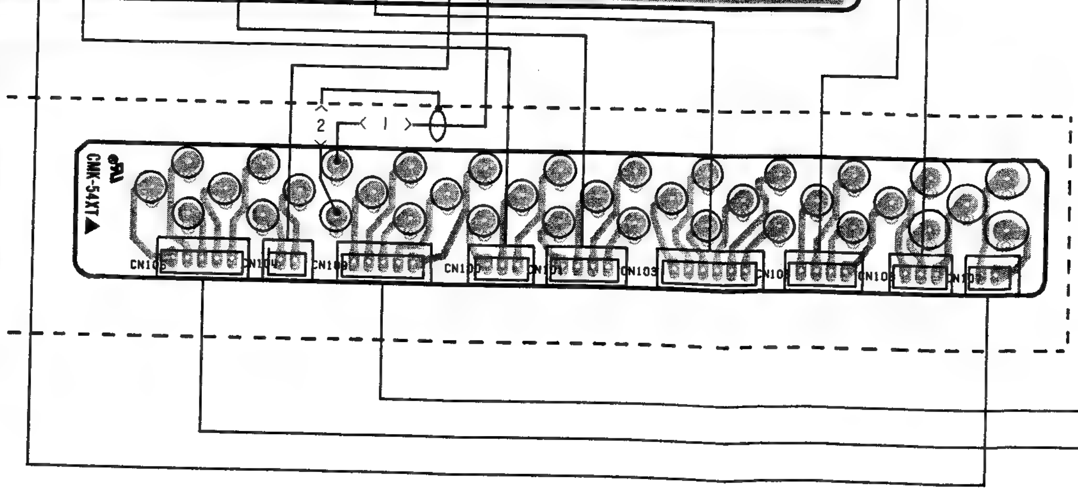
This P.C.B. connection diagram is viewed from the parts mounted side.



THRU TYPE CAPACITORS ASSEMBLY



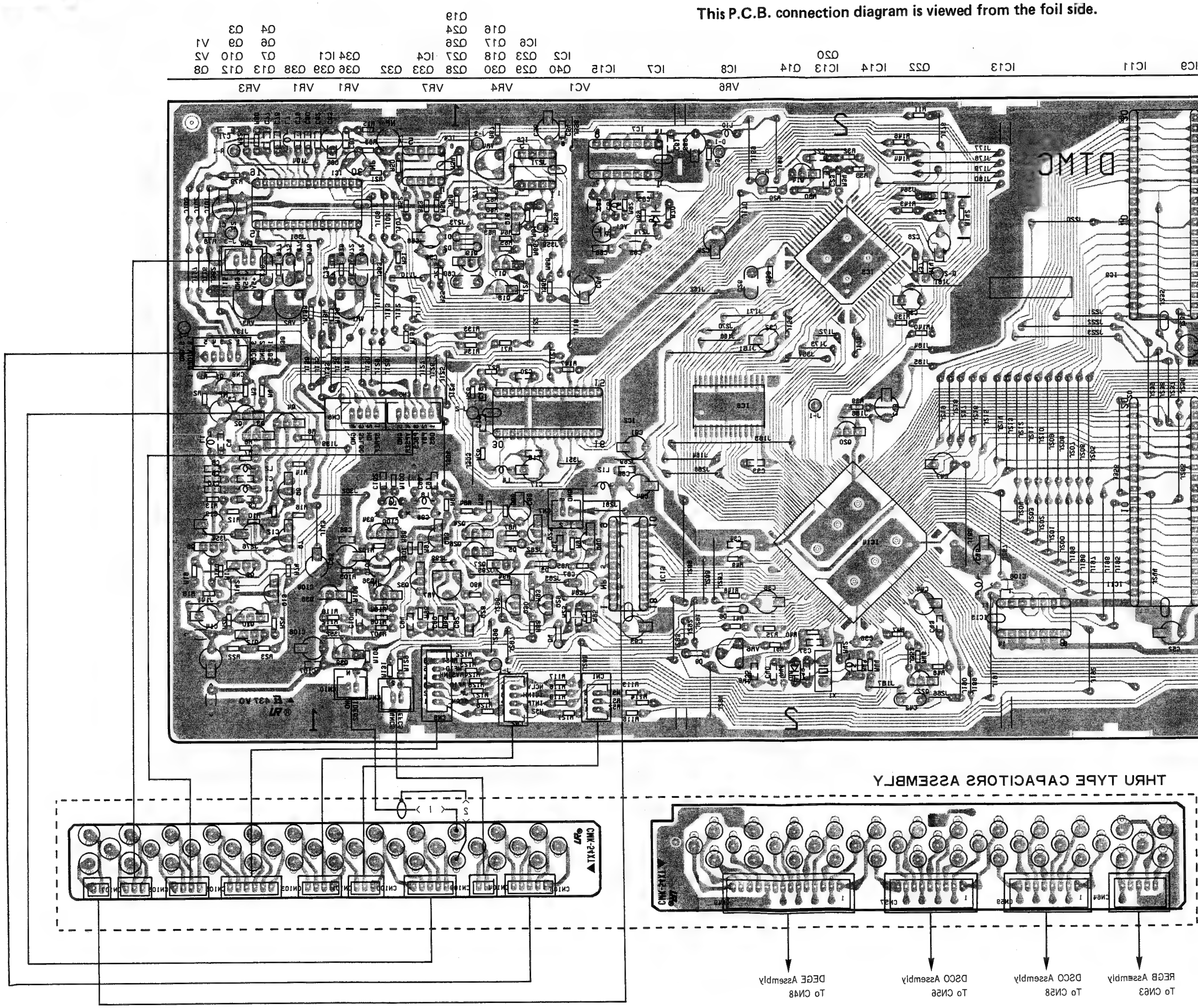




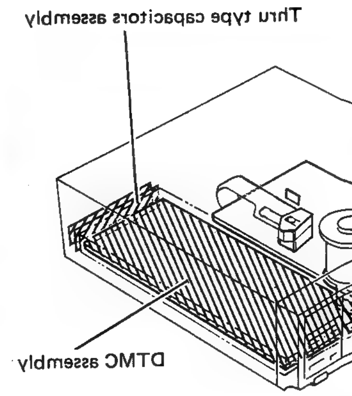
6 | 5 | 4 | 3 | 2 | 1

DTMC ASSEMBLY

This P.C.B. connection diagram is viewed from the foil side.

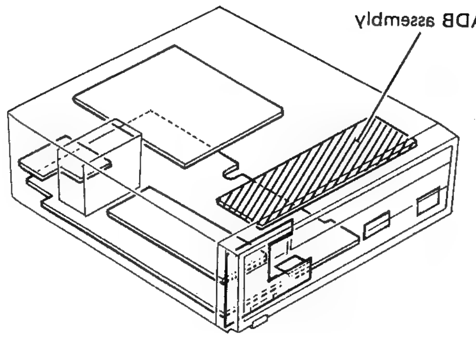


THRU TYPE CAPACITORS ASSEMBLY

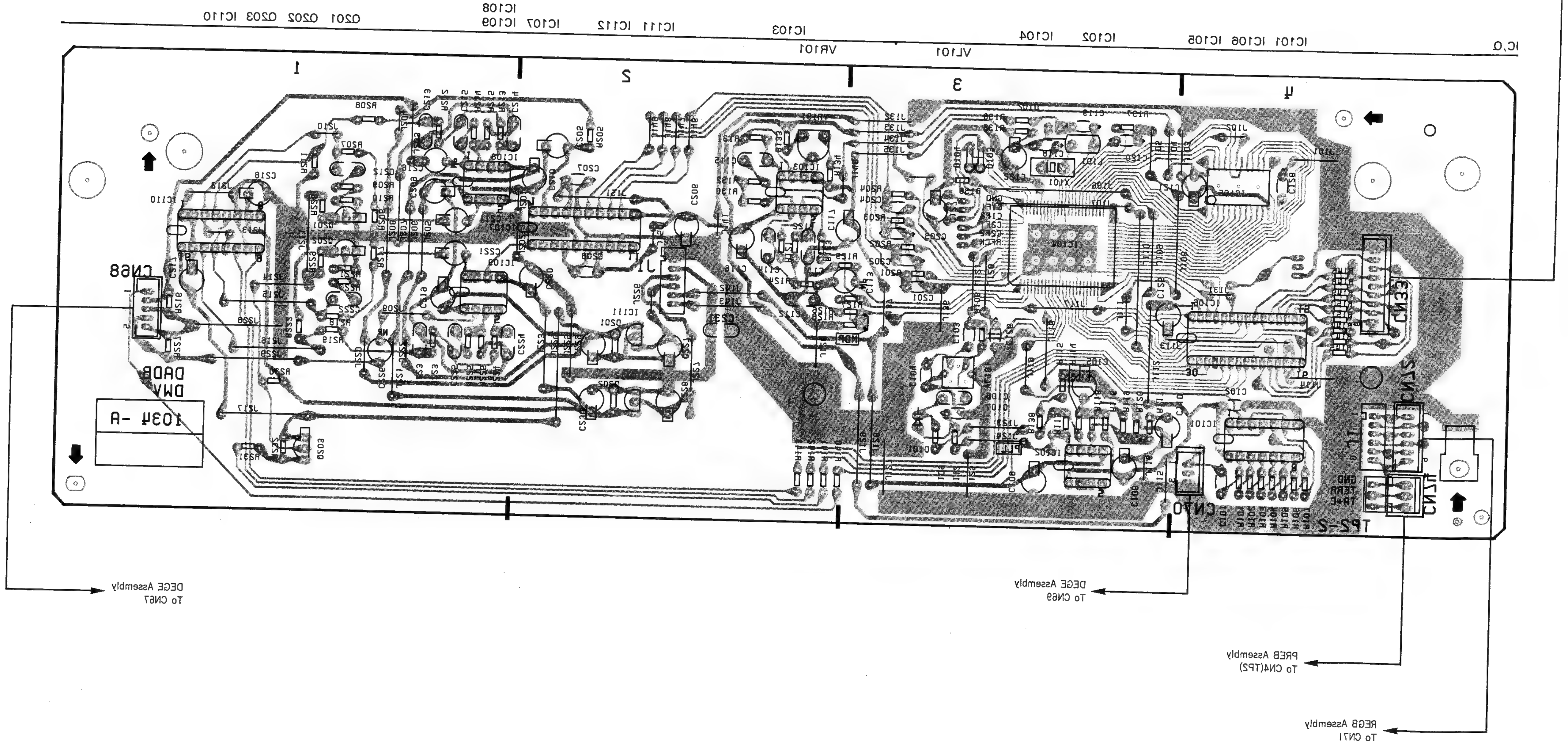


6 | 5 | 4 | 3 | 2 | 1

5. 5 DADB (DWV1034) ASSEMBLY

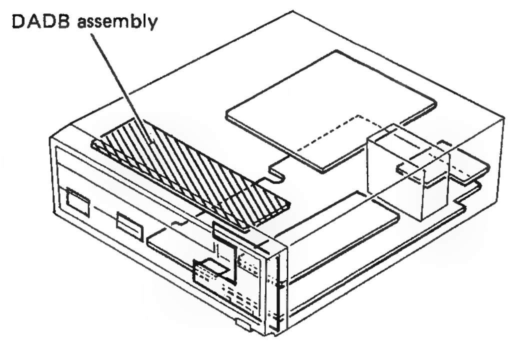


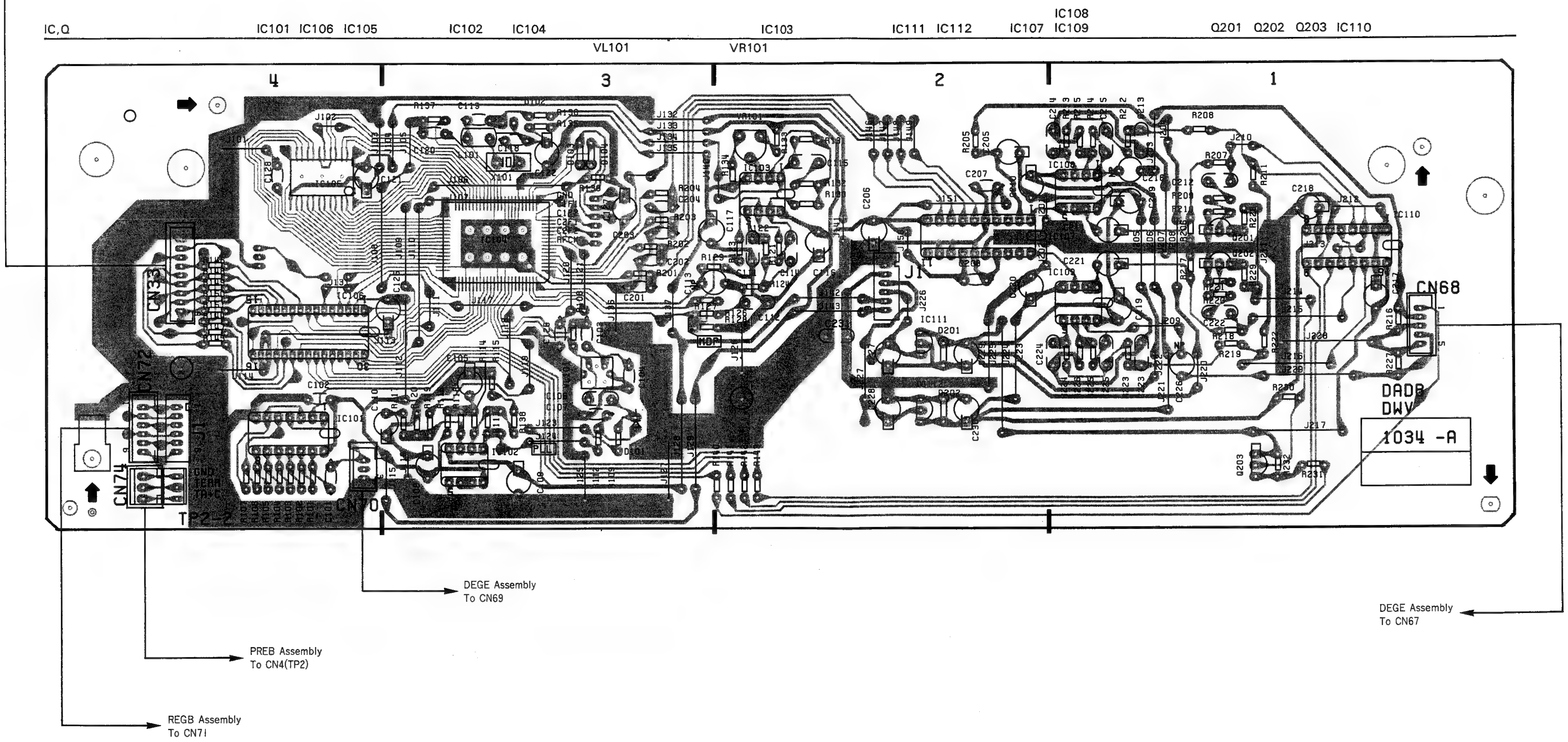
This P.C.B. connection diagram is viewed from the foil side.

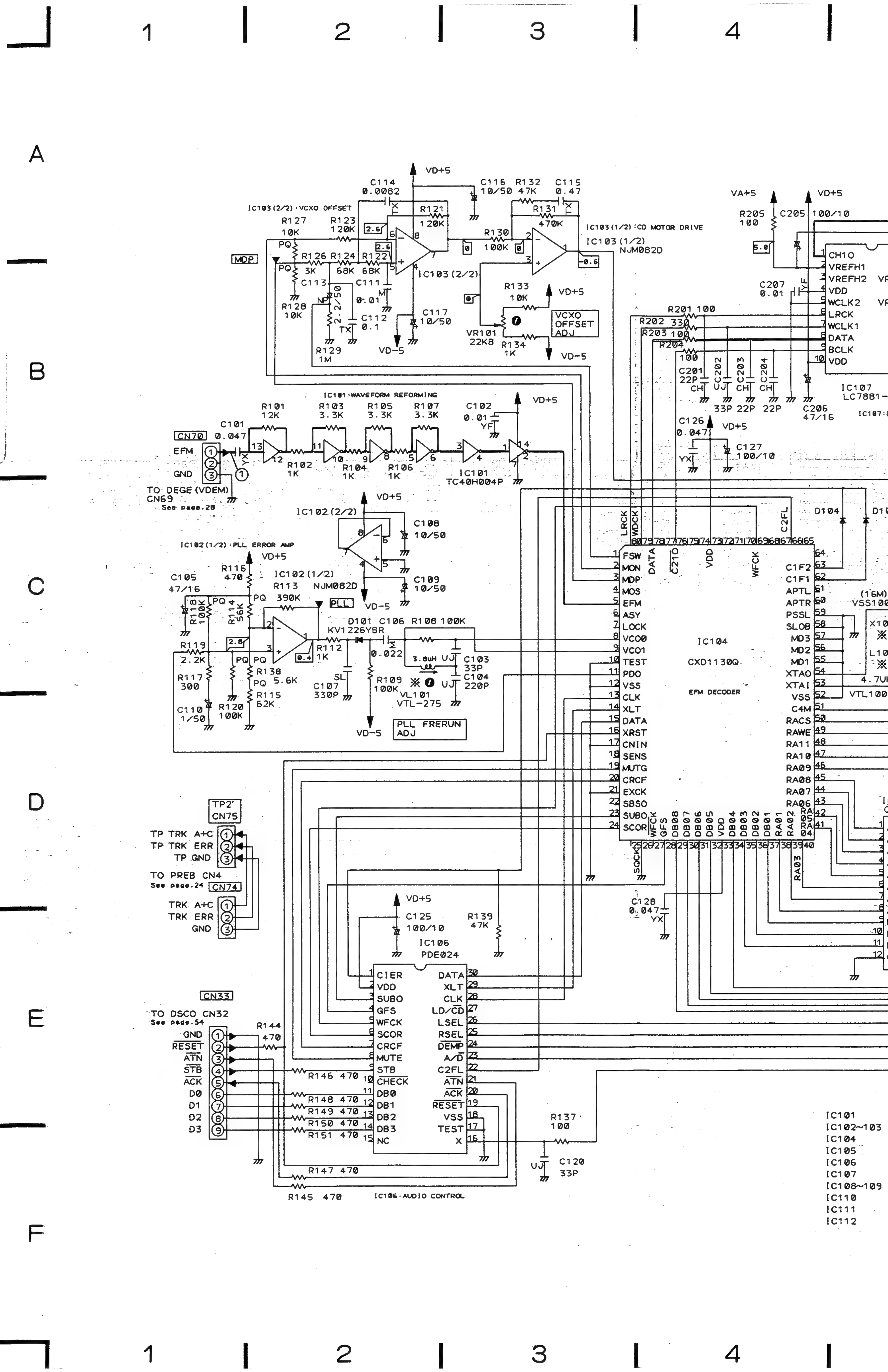


5. 5 DADB (DWV1034) ASSEMBLY

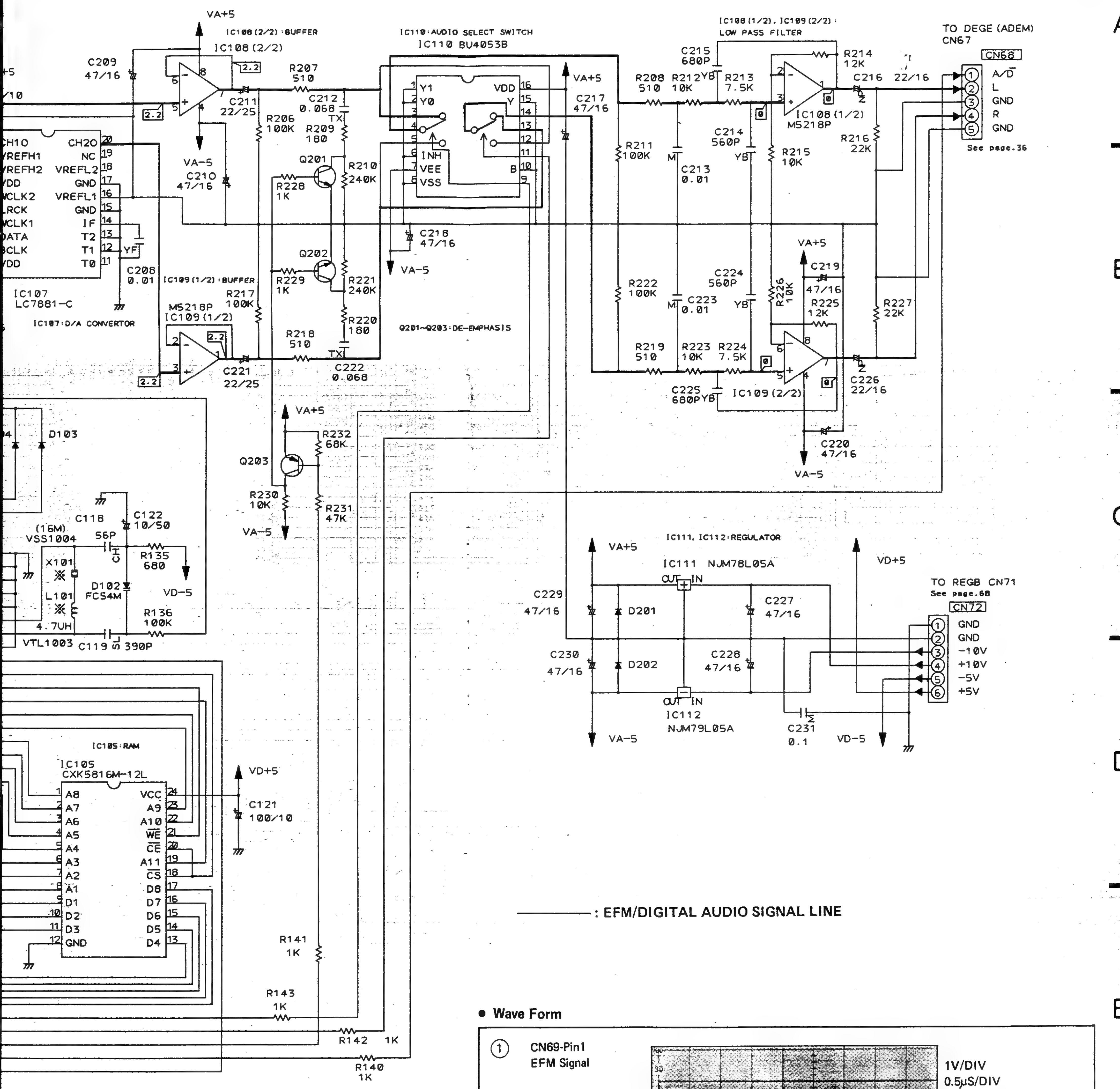
This P.C.B. connection diagram is viewed from the parts mounted side.







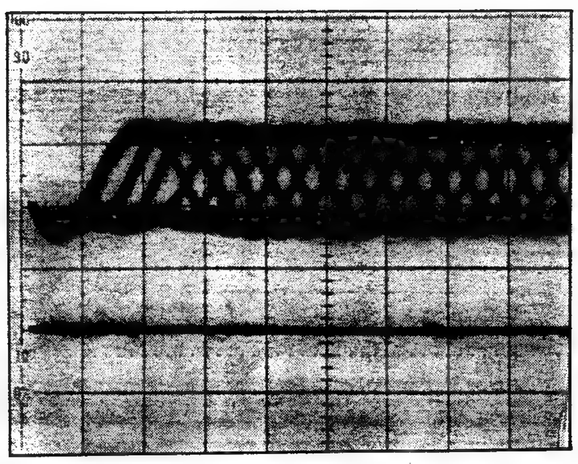
1
2
3
4
A
B
C
D
E
F
IC103(2/2):VCXO OFFSET
IC103(1/2):CD MOTOR DRIVE
IC103(1/2)
NJM082D
IC103(2/2)
VCXO OFFSET ADJ
VR101 22KB
MDP
VD+5
VD-5
VA+5
C114 0.0082
C116 10/50
R132 47K
C115 0.47
R127 10K
R123 120K
R121 120K
R131 470K
R130 100K
R126 3K
R124 68K
R122 68K
R133 10K
R134 1K
R128 10K
R129 1M
C113 2.2/50
C111 0.01
C112 0.1
C117 10/50
IC101:WAVEFORM REFORMING
IC101
TC40H004P
CN70
EFM
GND
TO DEGE (VDEM) CN69
See page.28
C101 0.047
R101 12K
R103 3.3K
R105 3.3K
R107 3.3K
R102 1K
R104 1K
R106 1K
C102 0.01
IC102(2/2)
C108 10/50
C109 10/50
IC102(1/2):PLL ERROR AMP
IC102(1/2)
NJM082D
C105 47/16
R116 470
R113 390K
R118 100K
R114 56K
R119 2.2K
R117 300
C110 1/50
R120 100K
R138 5.6K
R115 62K
PLL
D101 KV1226YBR
C106 0.022
R108 100K
R112 1K
C107 330P
R109 100K
VL101 VTL-275
C103 33P
C104 220P
PLL FRERUN ADJ
R205 100
C205 100/10
C207 0.01
R201 100
R202 330
R203 100
R204 100
C201 22P
C202 33P
C203 22P
C204 22P
C206 47/16
C126 0.047
C127 100/10
IC107
LC7881
CH10
VREFH1
VREFH2
VDD
WCLK2
LRCK
WCLK1
DATA
BCLK
VDD
D104
IC104
CXD1130Q
EFM DECODER
FSW
MON
MDP
MOS
EFM
ASY
LOCK
VCO0
VCO1
TEST
PDO
VSS
CLK
XLT
DATA
XRST
CNIN
SENS
MUTG
CRCF
EXCK
SBSO
SUBO
SCOR
C1F2
C1F1
APTL
APTR
PSSL
SLOB
MD3
MD2
MD1
XTAO
XTAI
VSS
C4M
RACS
RAWE
RA11
RA10
RA09
RA08
RA07
RA06
RA05
RA04
RA03
RA02
RA01
LRCK
WDCK
DATA
C210
VDD
WFCK
C2FL
SQCK
GFS
DB08
DB07
DB06
DB05
DB04
DB03
DB02
DB01
(16M)
VSS100
X10
L10
4.7U
VTL100
C128 0.047
TP2' CN75
TP TRK A+C
TP TRK ERR
TP GND
TO PREB CN4
See page.24
CN74
TRK A+C
TRK ERR
GND
C125 100/10
R139 47K
IC106
PDE024
CIER
VDD
SUBO
GFS
WFCK
SCOR
CRCF
MUTE
STB
CHECK
DB0
DB1
DB2
DB3
NC
DATA
XLT
CLK
LD/CD
LSEL
RSEL
DEMP
A/D
C2FL
ATN
ACK
RESET
VSS
TEST
X
CN33
TO DSCO CN32
See page.54
GND
RESET
ATN
STB
ACK
D0
D1
D2
D3
R144 470
R146 470
R148 470
R149 470
R150 470
R151 470
R147 470
R145 470
R137 100
C120 33P
IC106:AUDIO CONTROL
IC101
IC102~103
IC104
IC105
IC106
IC107
IC108~109
IC110
IC111
IC112



——— : EFM/DIGITAL AUDIO SIGNAL LINE

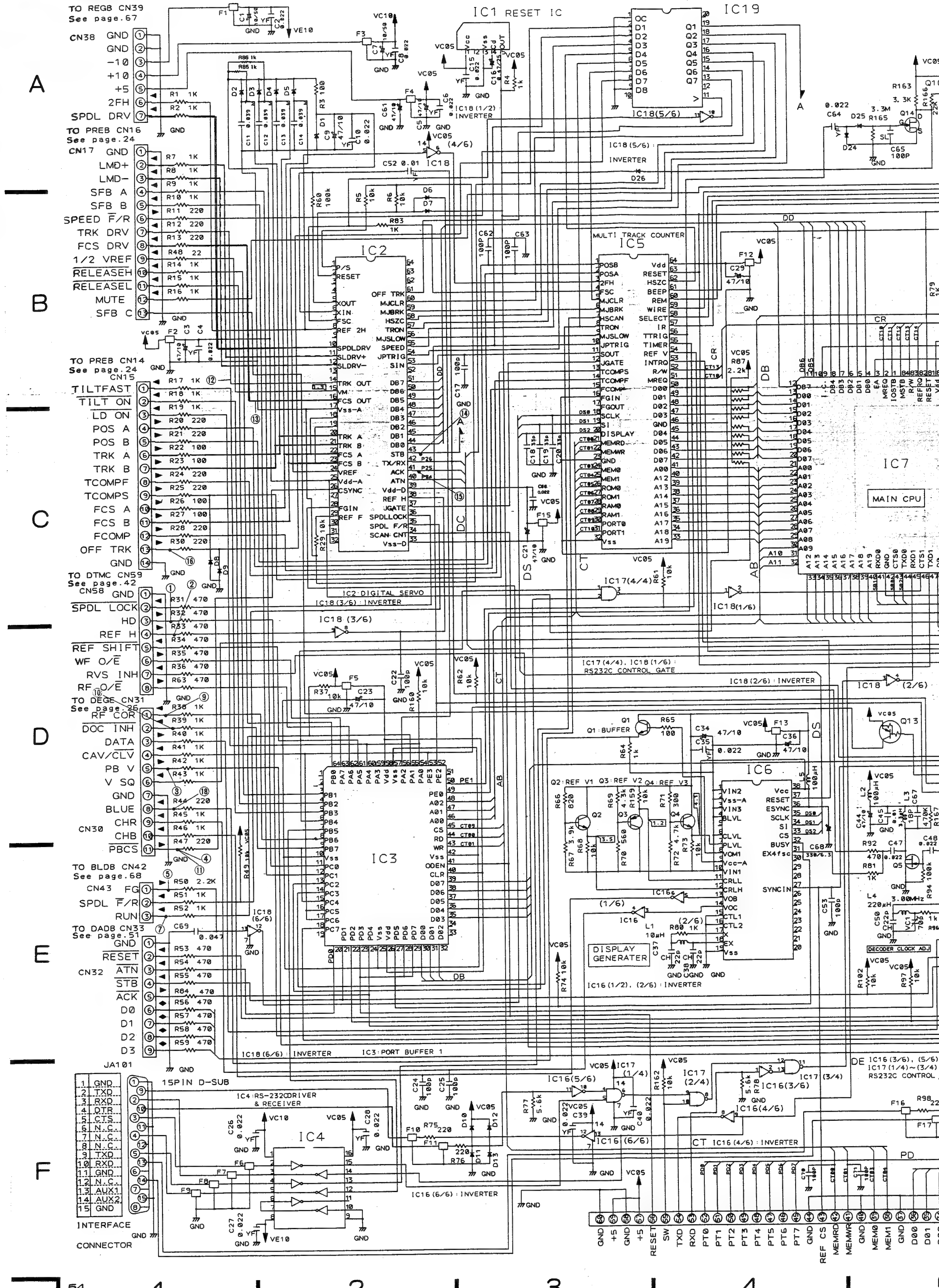
- **Wave Form**

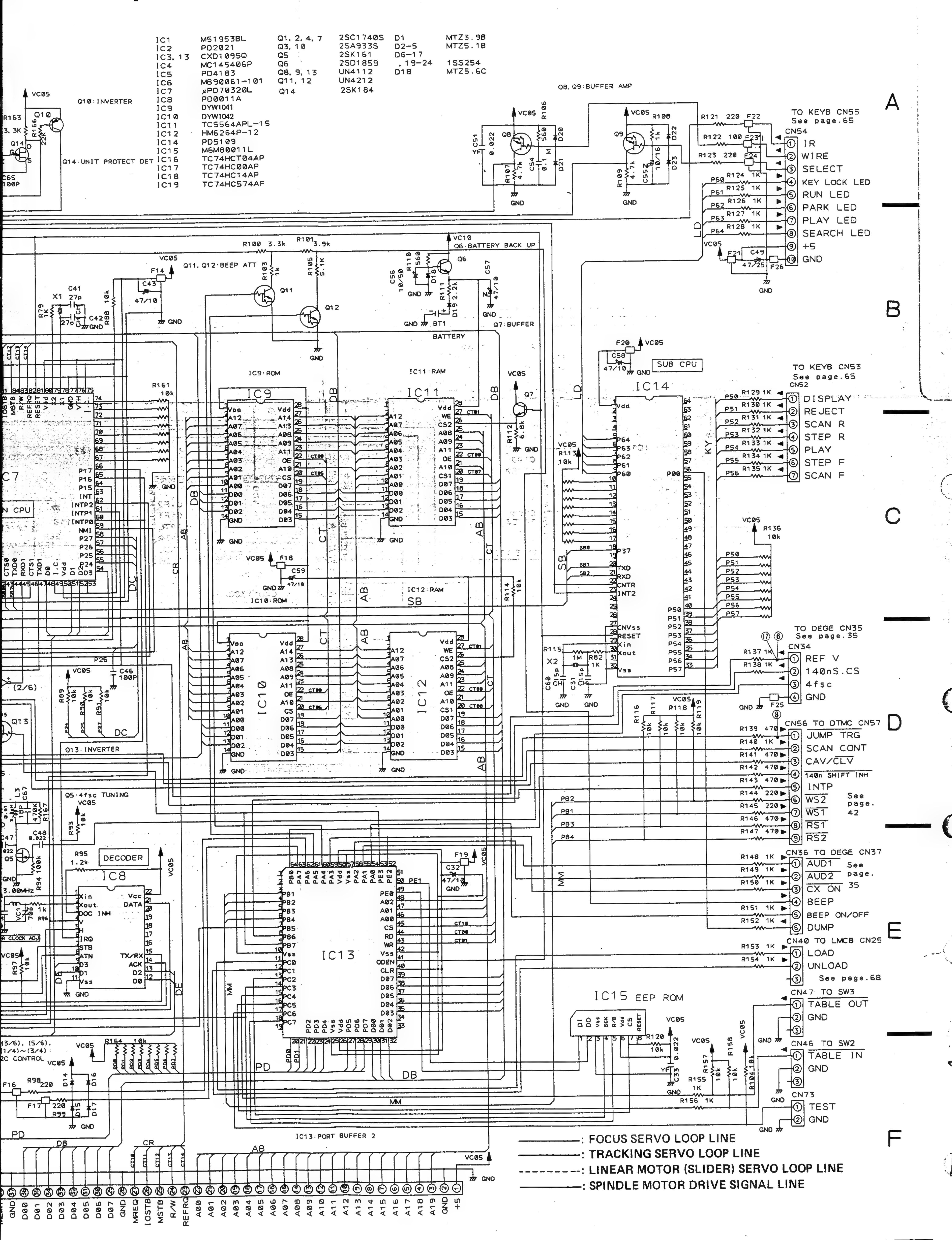
① CN69-Pin1
EFM Signal



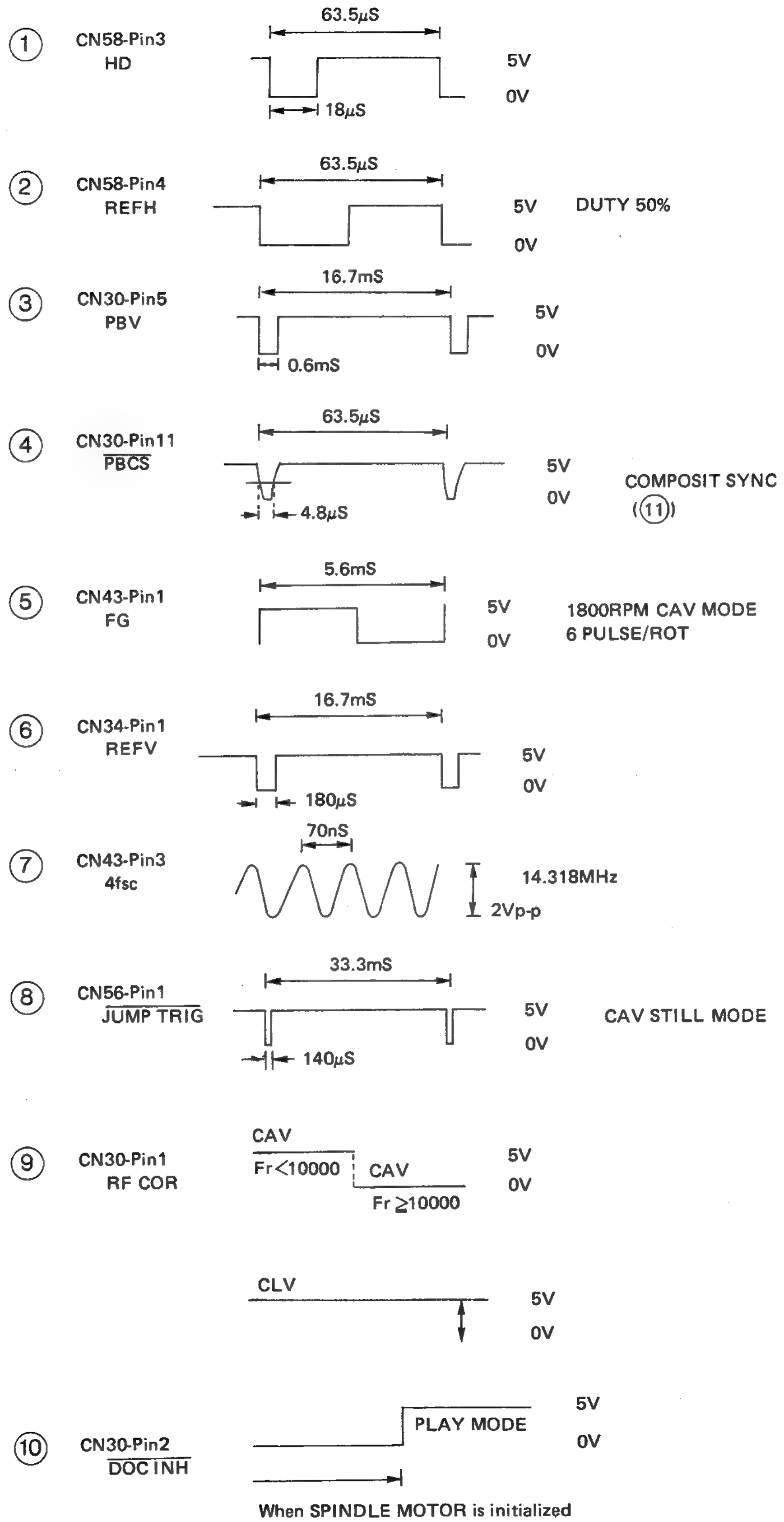
IC101	TC40H004P	Q201~202	2SC1740S
IC102~103	NJM082D	Q203	2SA933S
IC104	CXD1130Q	D101	KV1225YBR
IC105	CXK5816M-12L	D102	FC54M
IC106	PDE024	D103~104	1SS254
IC107	LC7881-C	D201~202	1SS254
IC108~109	M5218P	L101	VTL1003
IC110	BU4053B	VL101	VTL-275
IC111	NJM78L05A	VR101	VRTB6VS223
IC112	NJM79L05A	X101	VSS1004

5. 6 DSCO (DWG1076) ASSEMBLY



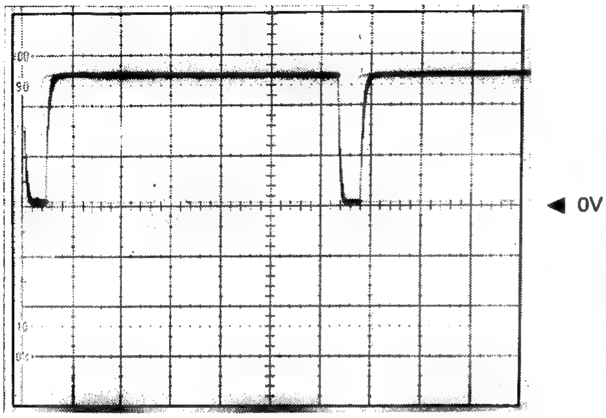

IC1 M51953BL
IC2 PD2021
IC3, 13 CXD1095Q
IC4 MC145406P
IC5 PD4183
IC6 MB90061-101
IC7 μPD70320L
IC8 PD0011A
IC9 DYW1041
IC10 DYW1042
IC11 TC5564APL-15
IC12 HM6264P-12
IC14 PD5109
IC15 M6M80011L
IC16 TC74HCT04AP
IC17 TC74HC00AP
IC18 TC74HC14AP
IC19 TC74HC574AF
Q1, 2, 4, 7 2SC1740S
Q3, 10 2SA933S
Q5 2SK161
Q6 2SD1859
Q8, 9, 13 UN4112
Q11, 12 UN4212
Q14 2SK184
D1 MTZ3.9B
D2-5 MTZ5.1B
D6-17, 19-24 1SS254
D18 MTZ5.6C
Q8, Q9: BUFFER AMP
Q10: INVERTER
Q14: UNIT PROTECT DET
Q11, Q12: BEEP ATT
Q6: BATTERY BACK UP
Q7: BUFFER
BATTERY
IC9: ROM
IC10: ROM
IC11: RAM
IC12: RAM
SUB CPU
IC14
IC13
IC13: PORT BUFFER 2
IC15 EEP ROM
DECODER
IC8
Q5: 4fsc TUNING
Q13: INVERTER
TO KEYB CN55 See page.65
CN54
IR
WIRE
SELECT
KEY LOCK LED
RUN LED
PARK LED
PLAY LED
SEARCH LED
+5
GND
TO KEYB CN53 See page.65
CN52
DISPLAY
REJECT
SCAN R
STEP R
PLAY
STEP F
SCAN F
TO DEGE CN35 See page.35
CN34
REF V
140nS.CS
4fsc
GND
CN56 TO DTMC CN57
JUMP TRG
SCAN CONT
CAV/CLV
140n SHIFT INH
INTP
WS2
WS1
RS1
RS2
See page. 42
CN36 TO DEGE CN37
AUD1
AUD2
CX ON
BEEP
BEEP ON/OFF
DUMP
See page. 35
CN40 TO LMCB CN25
LOAD
UNLOAD
See page.68
CN47 TO SW3
TABLE OUT
GND
CN46 TO SW2
TABLE IN
GND
CN73
TEST
GND
: FOCUS SERVO LOOP LINE
: TRACKING SERVO LOOP LINE
: LINEAR MOTOR (SLIDER) SERVO LOOP LINE
: SPINDLE MOTOR DRIVE SIGNAL LINE

- **Wave Forms**



1 CN58-Pin3 HD
63.5μS
18μS
5V
0V
2 CN58-Pin4 REFH
63.5μS
5V
0V
DUTY 50%
3 CN30-Pin5 PBV
16.7mS
0.6mS
5V
0V
4 CN30-Pin11 PBCS
63.5μS
4.8μS
5V
0V
COMPOSIT SYNC
(11)
5 CN43-Pin1 FG
5.6mS
5V
0V
1800RPM CAV MODE
6 PULSE/ROT
6 CN34-Pin1 REFV
16.7mS
180μS
5V
0V
7 CN43-Pin3 4fsc
70nS
14.318MHz
2Vp-p
8 CN56-Pin1 JUMP TRIG
33.3mS
140μS
5V
0V
CAV STILL MODE
9 CN30-Pin1 RF COR
CAV
Fr<10000
CAV
Fr≧10000
5V
0V
CLV
5V
0V
10 CN30-Pin2 DOC INH
PLAY MODE
5V
0V
When SPINDLE MOTOR is initialized

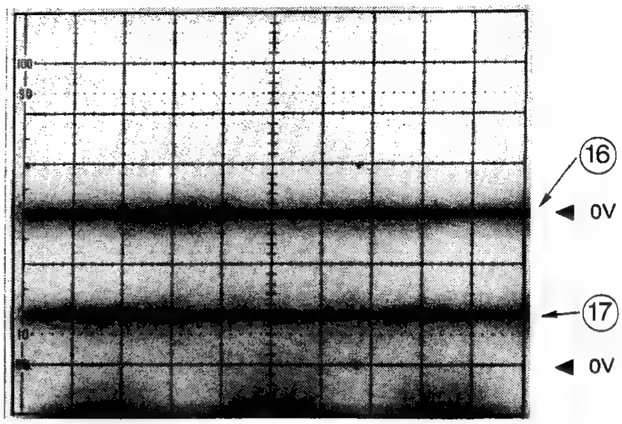
(11) CN30-Pin11: $\overline{\text{COMP SYNC}}$ 2V/div 10μS/div



(16) CN15-Pin13: OFF TRK 5V/div 5mS/div

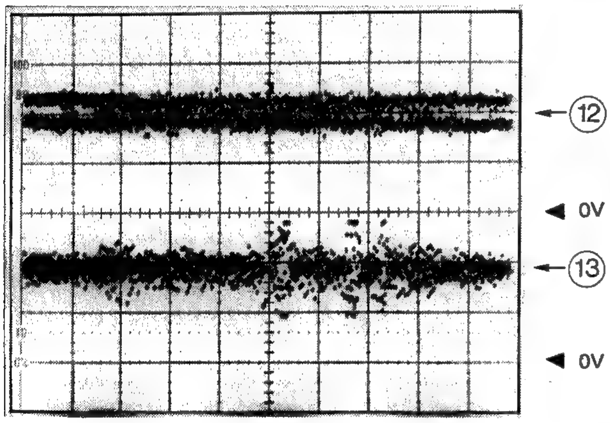
(17) CN56-Pin1: $\overline{\text{JUMP TRG}}$ 5V/div

STILL MODE: CAV DISC-STILL



(12) IC2-Pin14: TRK DRIVE 1V/div 5mS/div

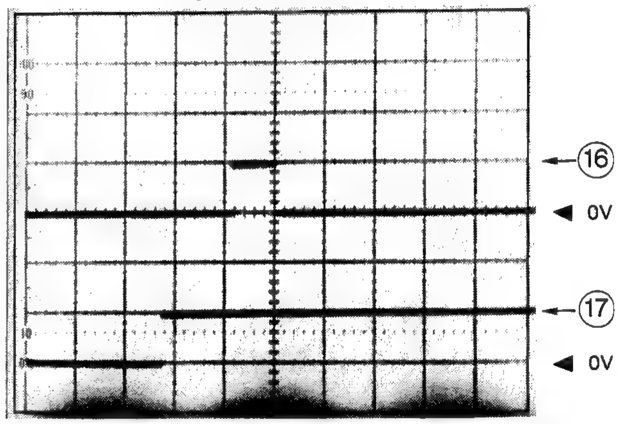
(13) IC2-Pin16: FOCUS DRIVE 1V/div



(16) CN15-Pin13: OFF TRK 5V/div 50μS/div

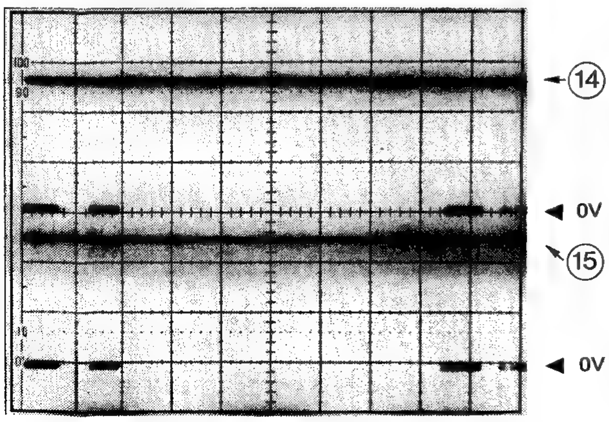
(17) CN56-Pin1: JUMP TRG 5V/div

(Enlargement of above photo)

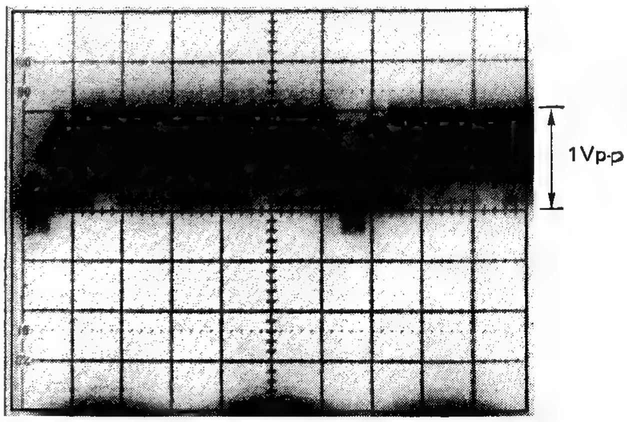


(14) IC2-Pin43: STB 2V/div 5mS/div

(15) IC2-Pin41: ACK 2V/div

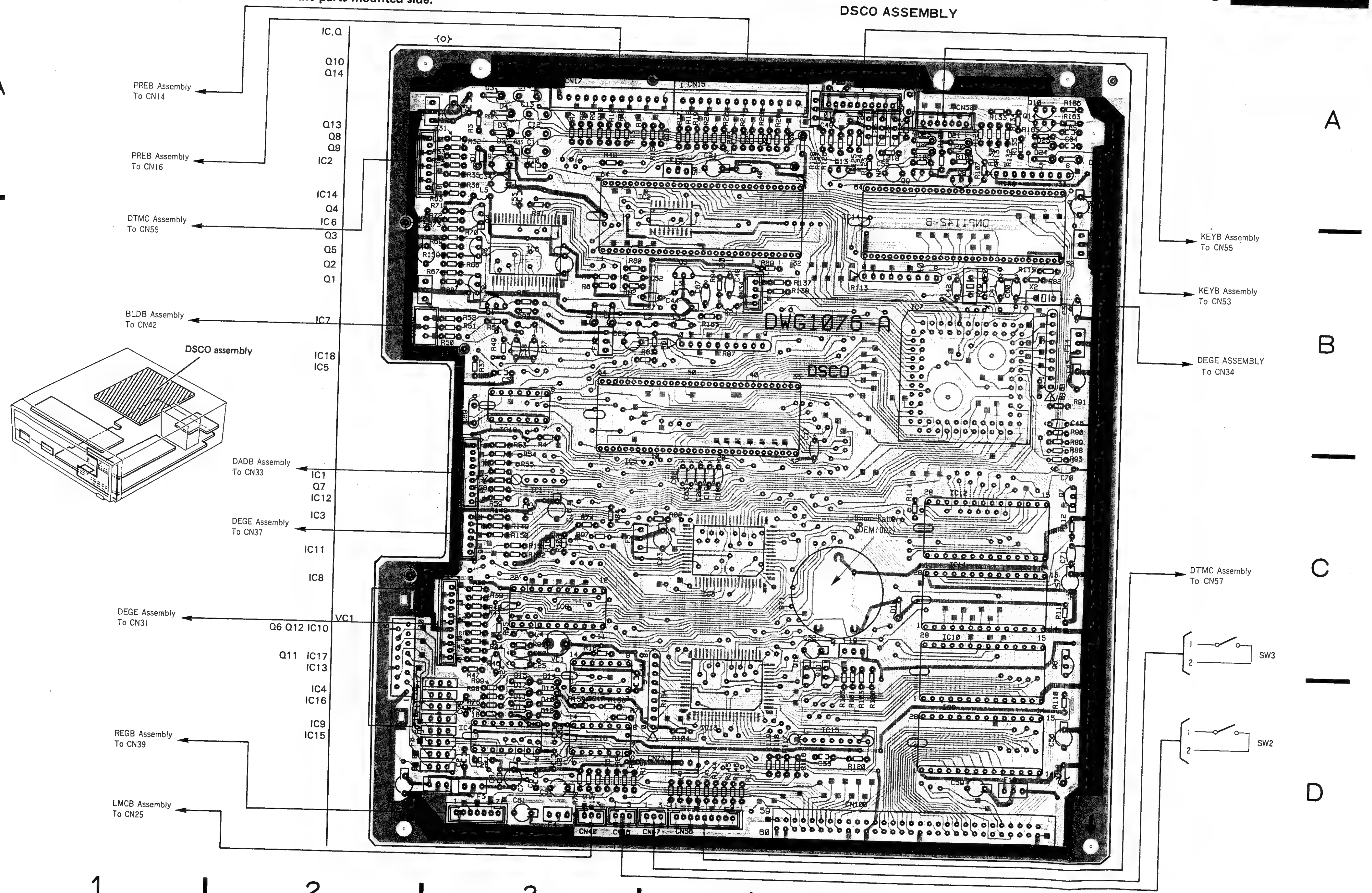


(18) CN30-Pin8: BLUE 0.5V/div 10μS/div

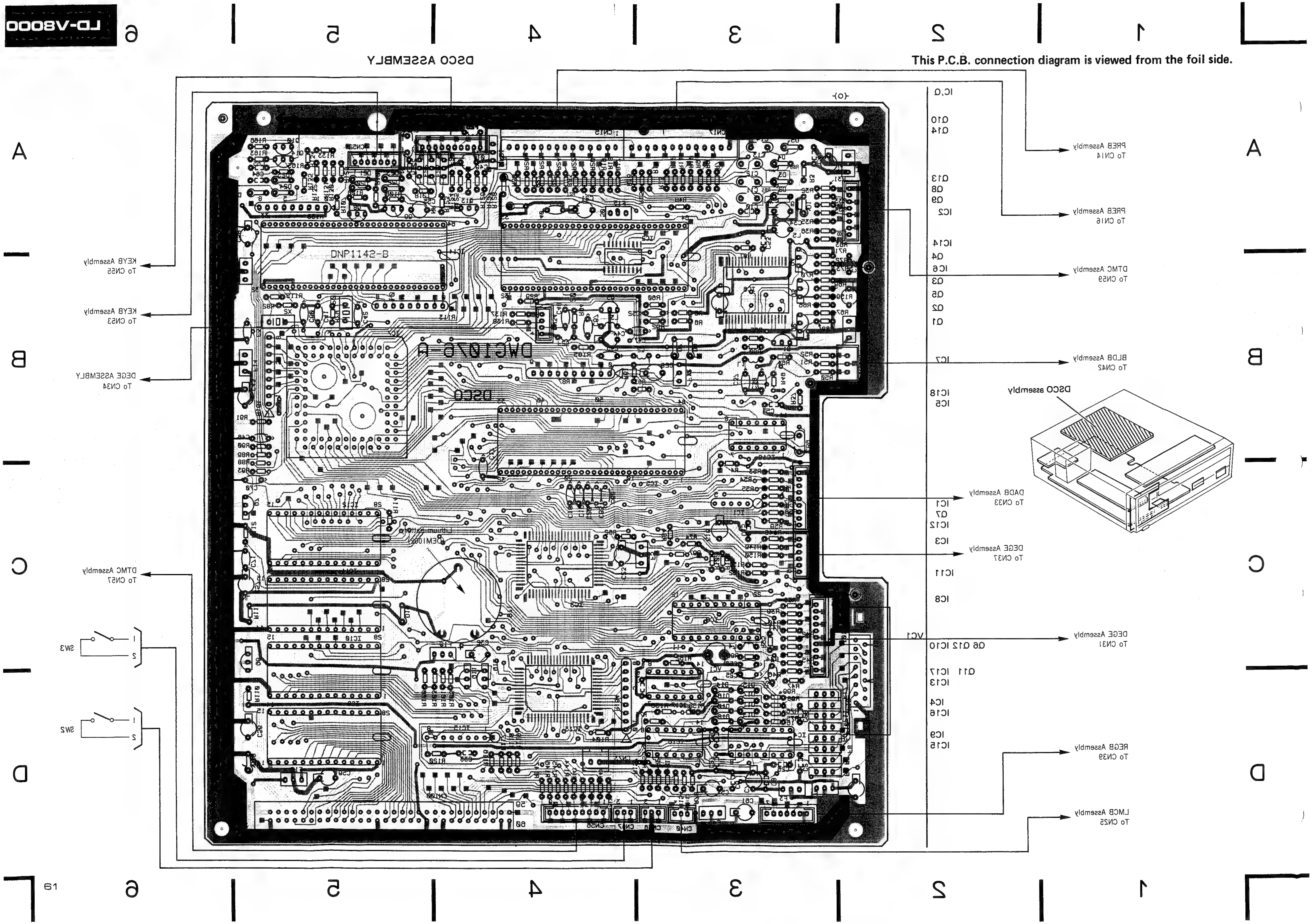


This P.C.B. connection diagram is viewed from the parts mounted side.

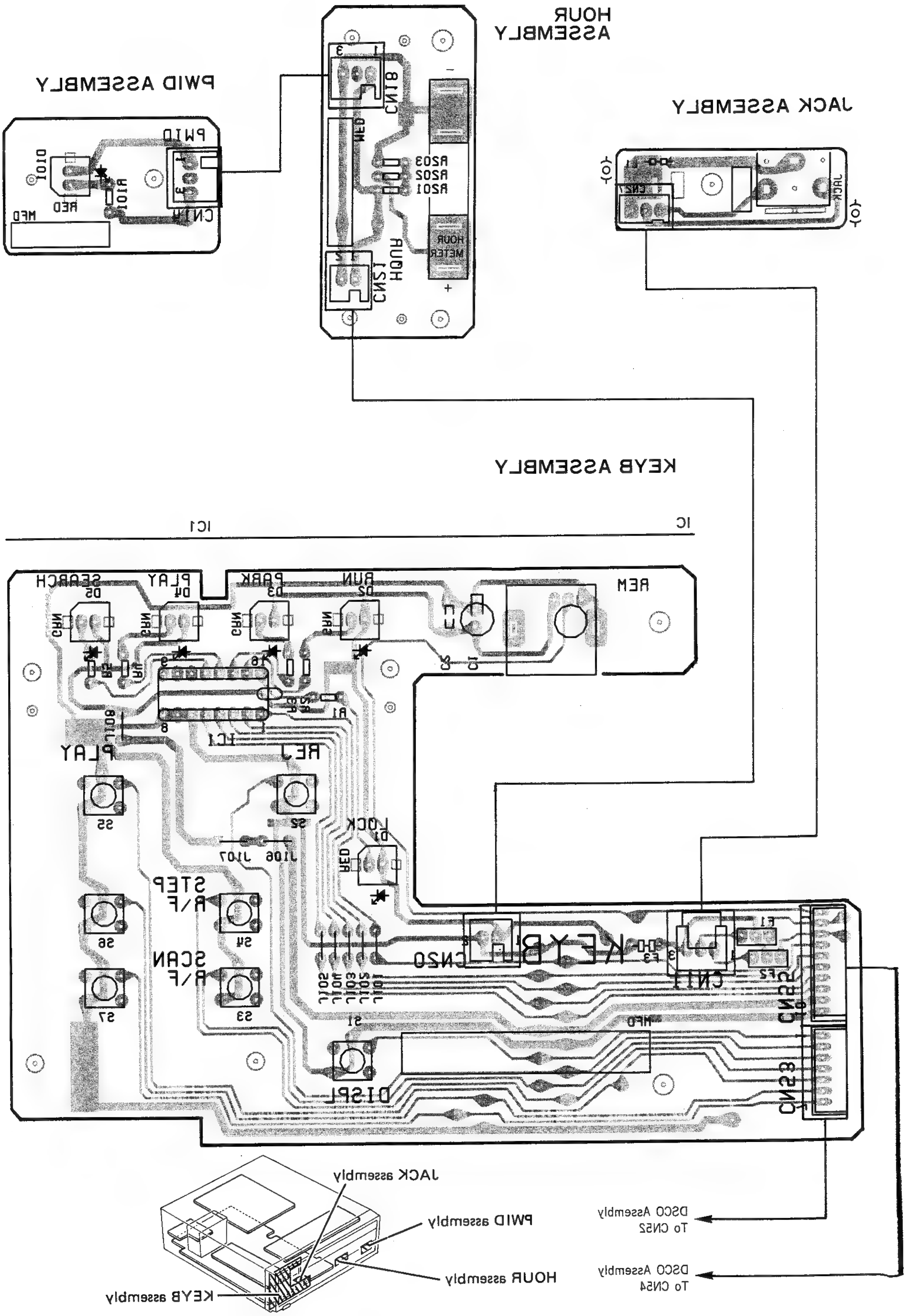
DSCO ASSEMBLY



This P.C.B. connection diagram is viewed from the foil side.

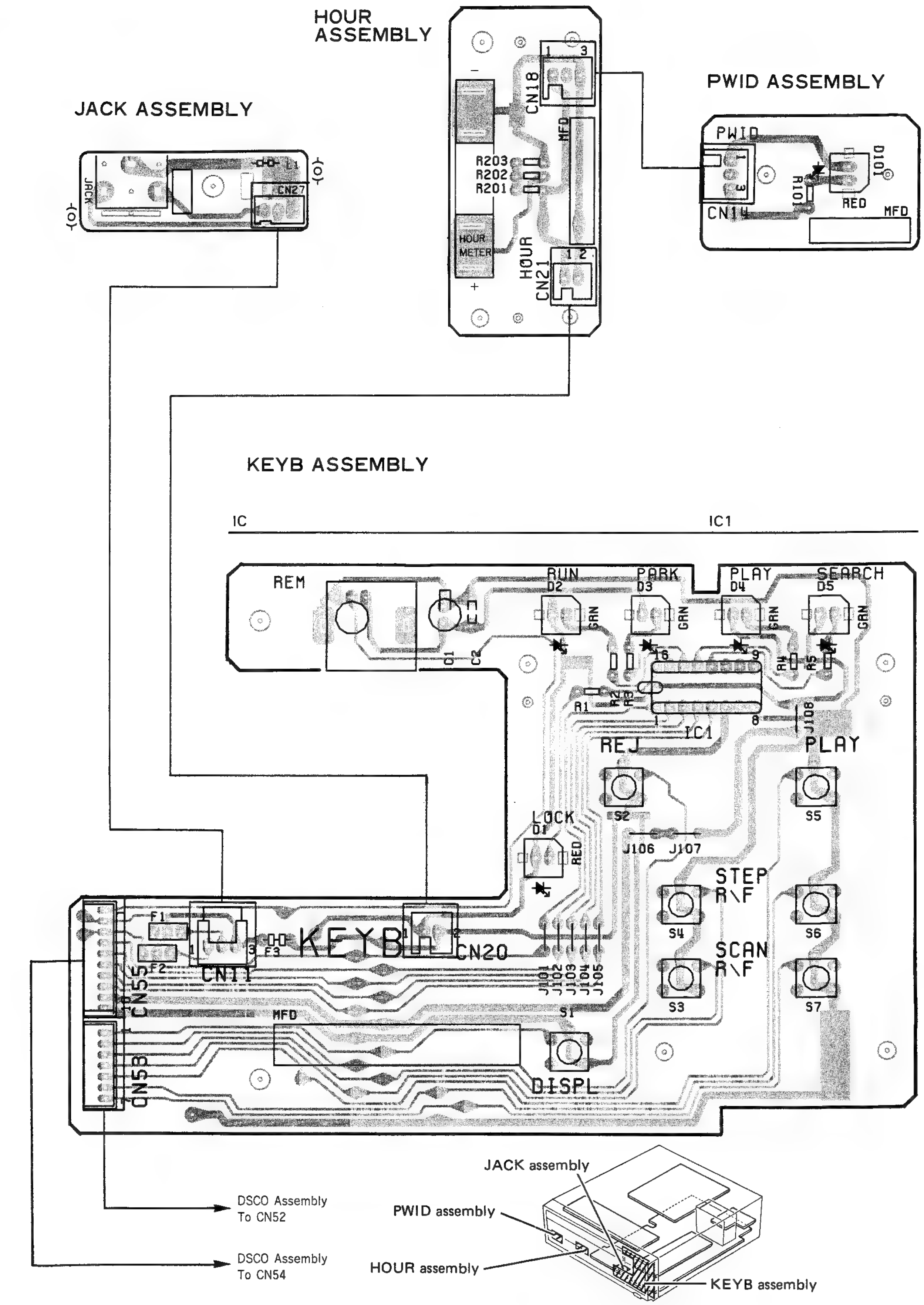


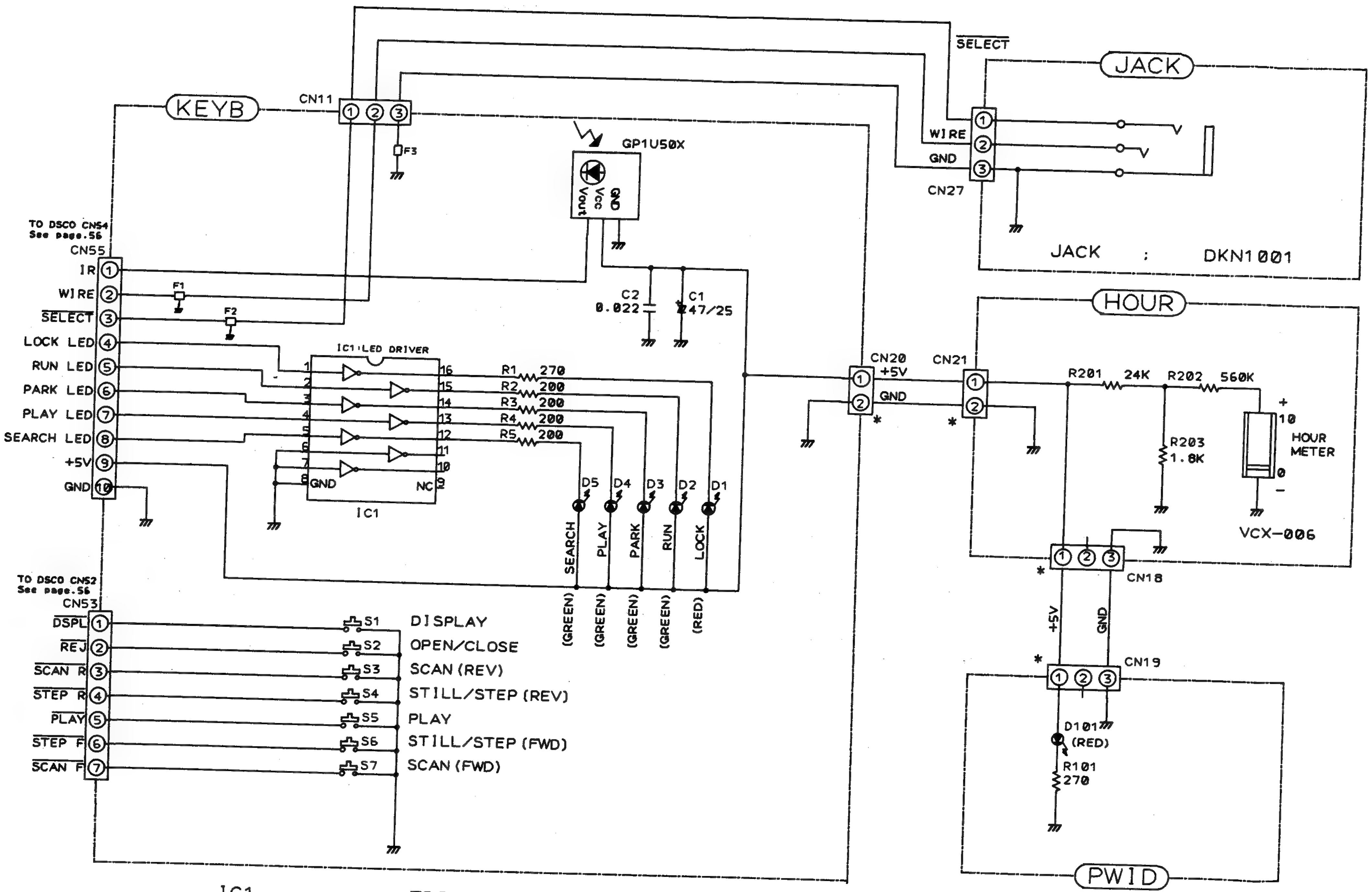
This P.C.B. connection diagram is viewed from the foil side.



5.7 KEYB, HOUR, PWID AND JACK ASSEMBLIES

This P.C.B. connection diagram is viewed from the parts mounted side.

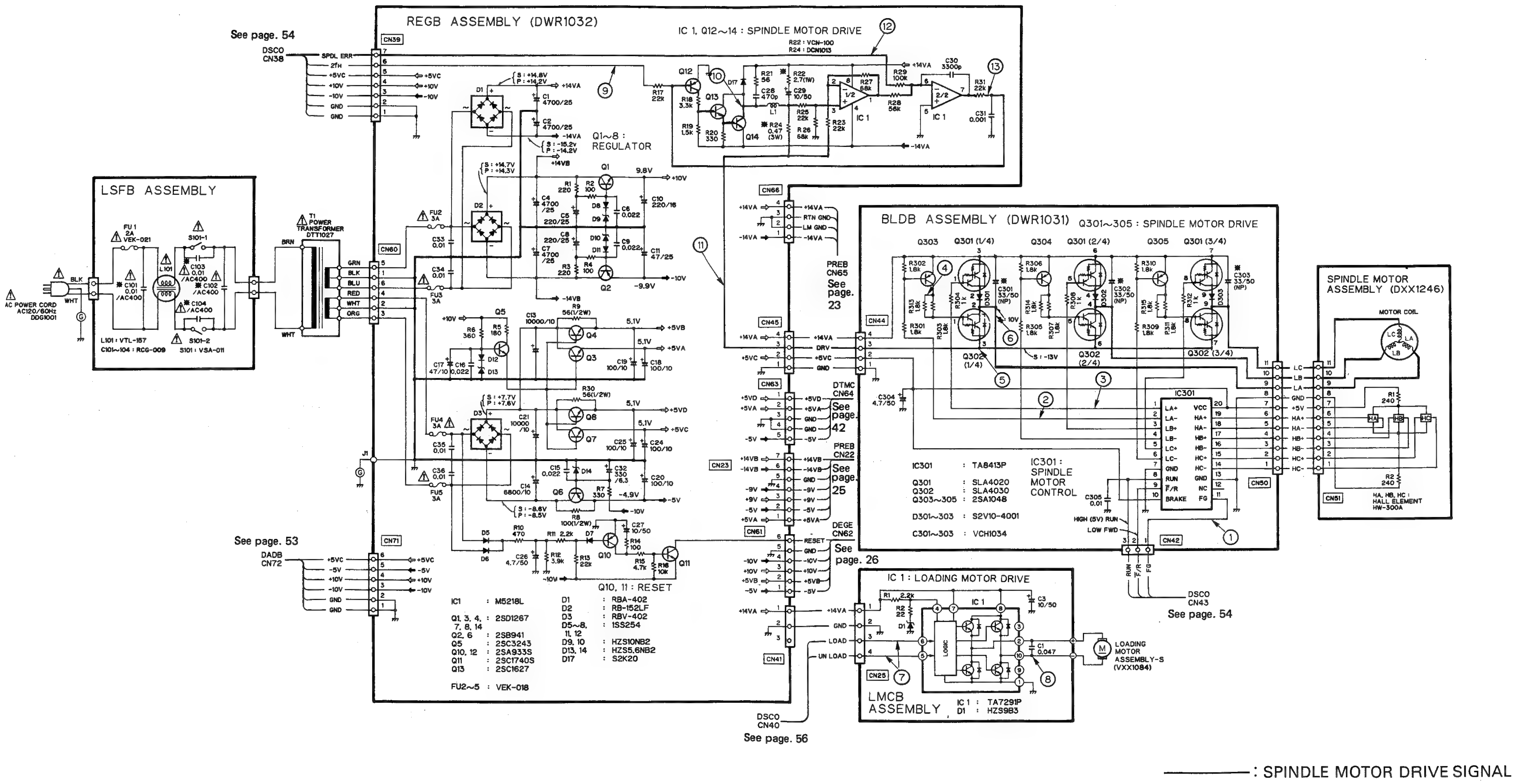




IC1	:	TD62504P
S1–S7	:	VSC-012
D1, D101	:	SLH-56VC3H-S
D2–D5	:	SLH-56MC3H-S
F1, F2	:	VTH1011
F3	:	DTF1003

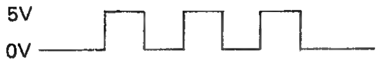
* Boardin Connector

5.8 REGB (DWR1032), LSFB, LMCB AND BLDB (DWR1031) ASSEMBLIES



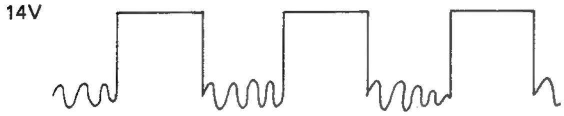
● Wave Forms

(1) IC301-Pin11 BLDB
PLAY:

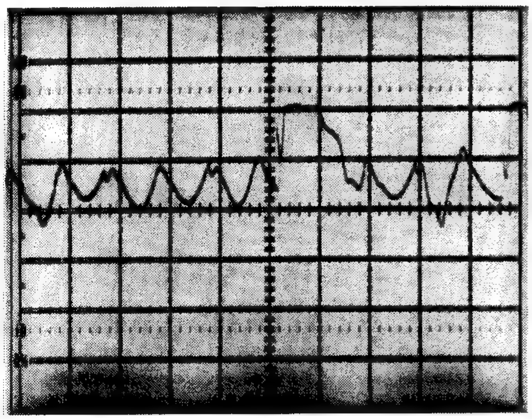


(2) IC301-Pin2
(3) IC301-Pin1
STAND BY: 16V
PLAY:

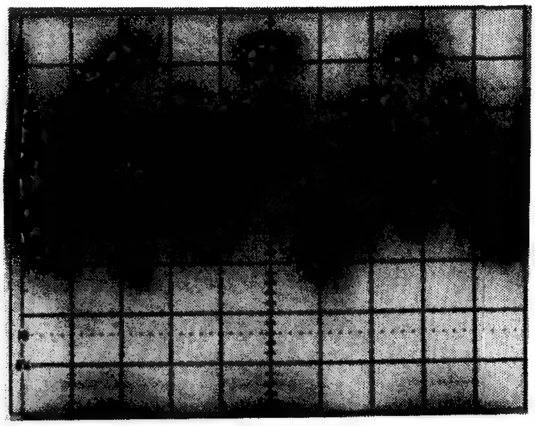
(4) Q303-C
PLAY:



(5) Q302-Pin3 BLDB
STAND BY: −13V
PLAY:
5mS/div
5V/div

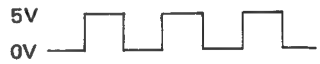


(6) Q302-Pin2 BLDB
STAND BY: 10V
PLAY:
10mS/div
5V/div

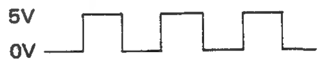


(7) CN25-Pin3,4 LMCB

When CLOSE: Both UNLOAD and LOAD will be high momentarily when starting.
Later, UNLOAD becomes (waveform) and LOAD becomes low, then just before close, both become high again.

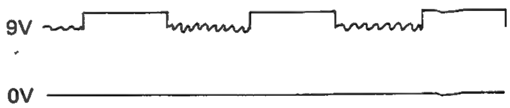


When OPEN: While operating, LOAD becomes (waveform) which is opposite the CLOSE waveform and UNLOAD becomes low, then both of them become high just before close.

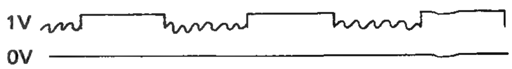


(8) IC1-Pin10 LMCB

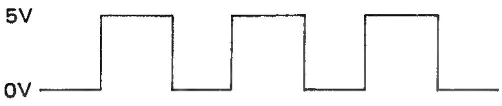
OPEN:



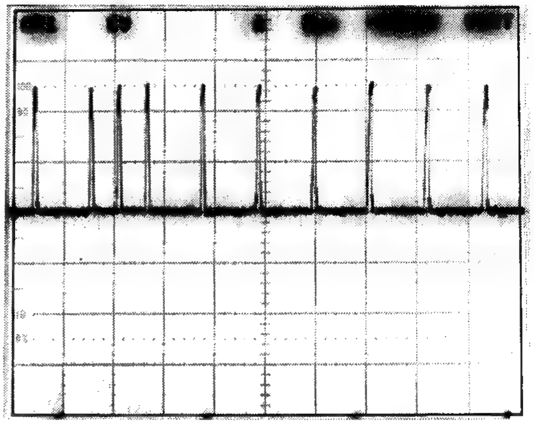
CLOSE:



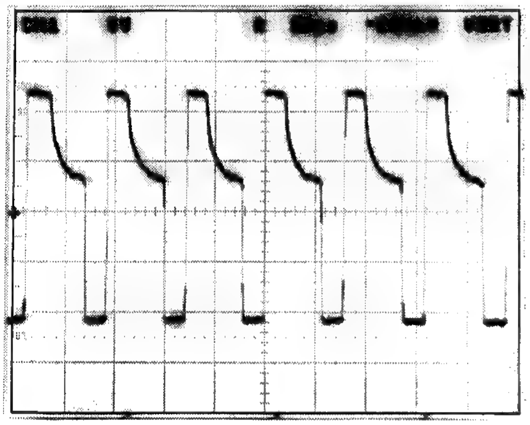
⑨ CN39-Pin6 SYPS
STAND BY and PLAY:



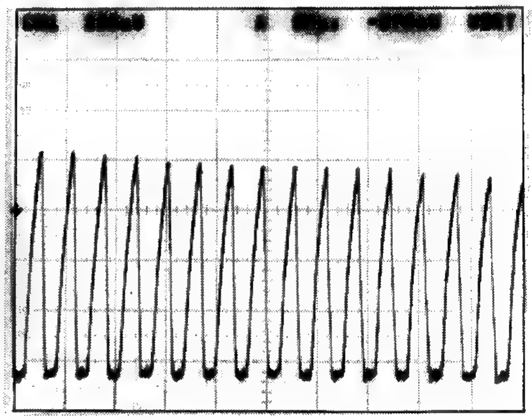
⑫ CN39-Pin7 2μS/div SYPS
PLAY: 2V/div



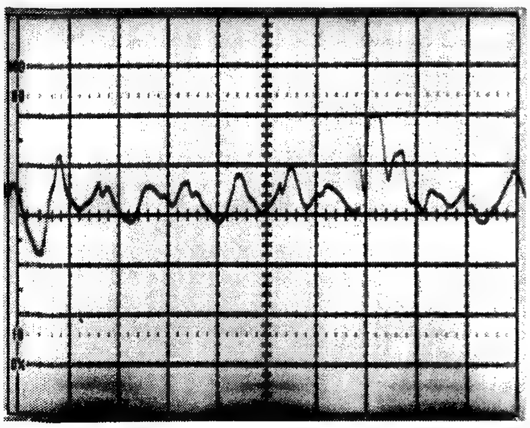
⑩ Q14-C 20μS/div SYPS
STAND BY: −12V 5V/div
PLAY:



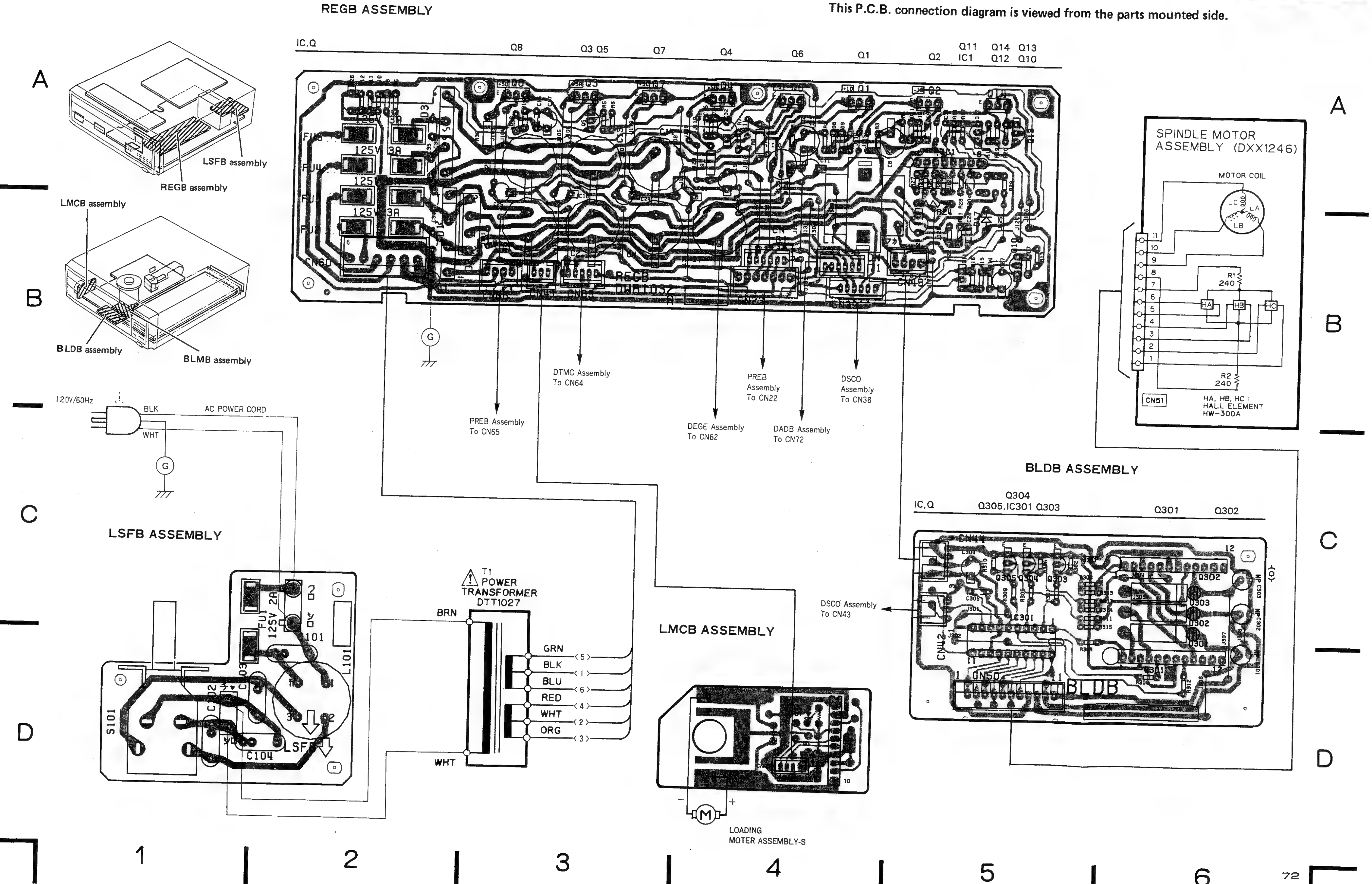
⑬ Q12-B 50μS/div SYPS
STAND BY: −3.5V 200mV/div
PLAY:



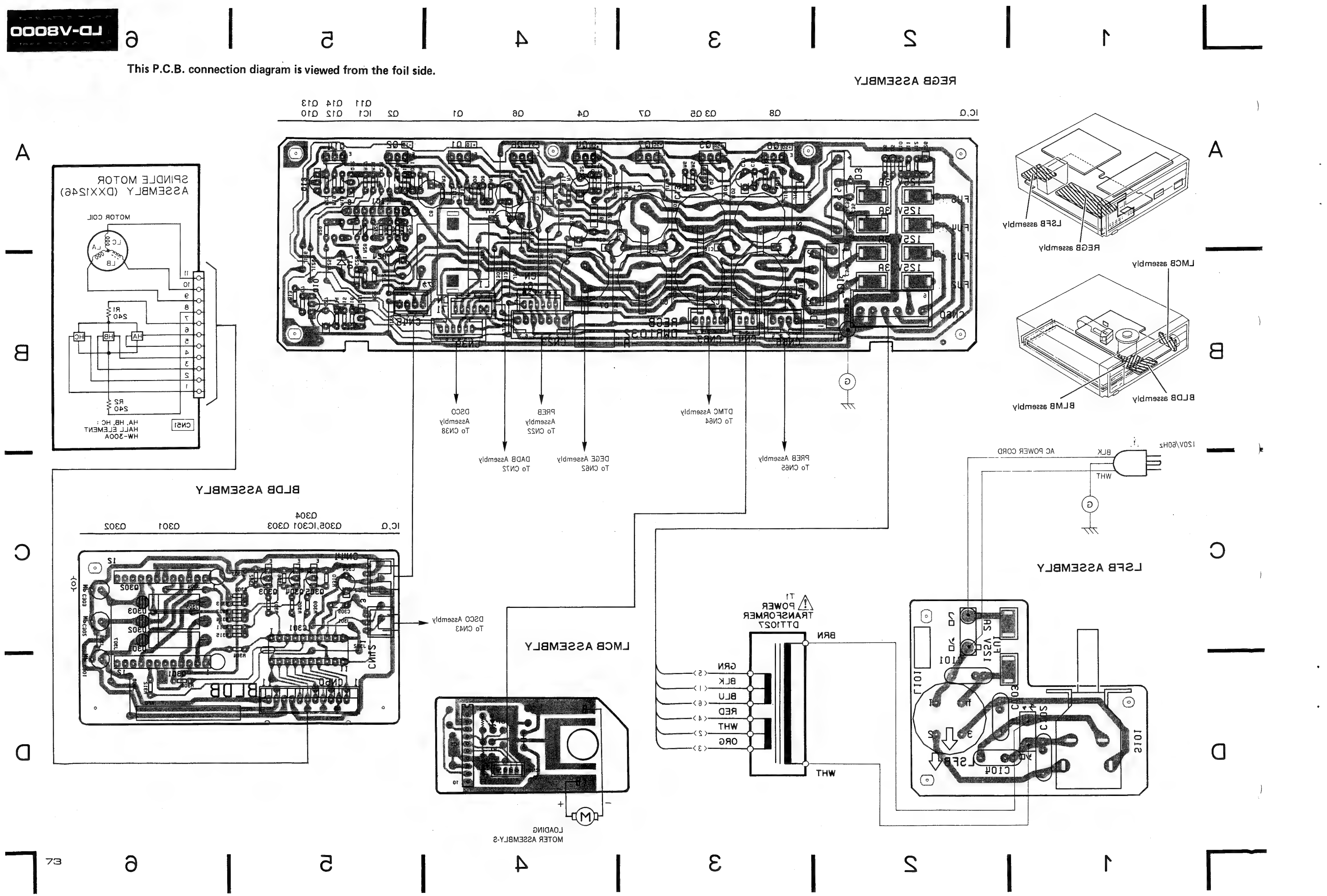
⑪ CN45-Pin3 5mS/div SYPS
STAND BY: −12V 5V/div
PLAY:



This P.C.B. connection diagram is viewed from the parts mounted side.



This P.C.B. connection diagram is viewed from the foil side.



6. ELECTRICAL PARTS LIST

NOTES:

- *Parts without part number cannot be supplied.*
- *Parts marked by "◉" are not always kept in stock. Their delivery time may be longer than usual or they may be unavailable.*
- *The ⚠ mark found on some component parts indicates the importance of the safety factor of the part. Therefore, when replacing, be sure to use parts of identical designation.*
- *When ordering resistors, first convert resistance values into code form as shown in the following examples.*

Ex. 1 *When there are 2 effective digits (any digit apart from 0), such as 560 ohm and 47k ohm (tolerance is shown by J = 5%, and K = 10%).*

560Ω	*56 × 10¹*	*561*	.........................*RD1/4PS* 5 6 1 *J*
47kΩ	*47 × 10³*	*473*	.........................*RD1/4PS* 4 7 3 *J*
0.5Ω	*0R5*		.........................*RN2H* 0 R 5 *K*
1Ω	*010*		.........................*RS1P* 0 1 0 *K*

Ex. 2 *When there are 3 effective digits (such as in high precision metal film resistors).*

5.62kΩ	*562 × 10¹*	*5621*	.........................*RN1/4SR* 5 6 2 1 *F*

Miscellaneous Parts

P.C. BOARD ASSEMBLIES

Mark	Symbol & Description	Part No.
	DSCO assembly	DWG1076
	JACK assembly	
	KEYB assembly	
	HOUR assembly	
	PWID assembly	
	REGB assembly	DWR1032
	LSFB assembly	
	DEGE assembly	DWV1033
	DADB assembly	DWV1034
	DTMC assembly	DWV1035
	BLDB assembly	DWR1031
	PREB assembly	DWV1032
	POSS assembly	
	HEAD assembly	
	LMCB assembly	
	Thru type capacitors assembly (This assembly is incorporated in DTMC assembly.)	DXX1248

OTHERS

Mark	Symbol	Description	Part No.
⚠		AC power cord	DDG1001
⚠	T1	Power transformer	DTT1027
	IC9	Program EPROM	DYW1041
	IC10	Program EPROM	DYW1042
		Hour meter	VCX-006
		Strain relief	VEC-201
⚠	FU2 – FU5	Fuse (3A)	VEK-018
⚠	FU1	Fuse (2A)	VEK-021
		Pick-up assembly	DWY1007
		Plunger	DXP1001
		Spindle motor assembly-S	DXX1246
		Tilt motor assembly-S	DXX1219
	M1	Loading motor assembly-S	VXX1084
	S2	Slide switch (TABLE/IN)	VSK-010
	S3	Slide switch (TABLE/OUT)	VSK-012

DSCO Assembly (DWG1076)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC3, IC13	CXD1095Q
	IC12	HM6264P-12
	IC6	MB90061-101
	IC4	MC145406P
	IC1	M51953BL
	IC15	M6M80011L
	IC8	PD0011A
	IC2	PD2021
	IC5	PD4183
	IC14	PD5109
	IC11	TC5564APL-15
	IC16	TC74HCT04AP
	IC17	TC74HC00AP
	IC18	TC74HC14AP
	IC7	μPD70320L-8
	IC19	TC74HC574AF
	Q8, Q9, Q13	UN4112
	Q11, Q12	UN4212
	Q3, Q10	2SA933S
	Q1, Q2, Q4, Q7	2SC1740S
	Q6	2SD1859
	Q5	2SK161
	Q14	2SK184
	D1	MTZ3.9B
	D2 – D5	MTZ5.1B
	D18	MTZ5.6C
	D6 – D17,D19 – D26	1SS254

COILS AND FILTERS

Mark	Symbol & Description		Part No.
	L1	Axial inductor	LAU100J
	L2	Axial inductor	LAU101J
	L3	Axial inductor	LAU3R3K
	L4	Axial inductor	LAU221J
	L5	Radial inductor	LRA101K
	F1 – F5, F12 – F15, F18 – F21	3 terminal filter	VTH1001
	F6 – F11, F16, F17, F22 – F24		VTH1011
	F25, F26	Ferrite bead	DTF1003

CAPACITORS

Mark	Symbol & Description		Part No.
	C31, C60		CCCCH150J50
	C37 C38, C50		CCCCH220J50
	C41 C42		CCCCH270J50
	C17, C22, C24, C25, C62, C63		CCCSL101J50
	C67		CCCCH180J50
	C18 – C20		CCCSL330J50
	C57		CEANL470M10
	C55		CEANP100M16
	C16		CEASR47M50
	C1, C7, C56		CEAS100M50
	C3, C5, C9, C21, C23, C29, C32, C34, C36, C43, C44, C49, C58, C59, C61		CEAS470M10
	C68		CEAS331M6R3
	C45, C52		CKCYF103Z50
	C70, C71, C46, C53, C65		CKPUYB101K50
	C2, C4, C6, C8, C10, C15, C26 – C28, C33, C35, C39, C40, C47, C48, C51, C64, C66		CKPUYF223Z25
	C54		CQMA104J50
	C11 – C14		CQMA393J50
	C69		CQMA473J50
	VC1	Ceramic trimmer (70pF)	VCM-009

RESISTORS

Mark	Symbol & Description		Part No.
	R113, R136, R161, R164	Resistor array (10kΩ × 8)	RA8S103J
	R87	Resistor array (2.2kΩ × 8)	RA9S222J
		Other resistors	RD1/6PM□□□J

OTHERS

Mark	Symbol & Description		Part No.
	BT1	Lithium battery	DEM1002
		84 pin IC socket	DKH1001
	X2	Crystal resonator	DSS1001
	X1	Crystal resonator	DSS1010
		IC socket	VKH-029
		28 pin IC socket	VKH1001
		D-SUB connector assembly (15 pin)	DXX1031

JACK Assembly

OTHER

Mark	Symbol & Description		Part No.
		Stereo mini jack	DKN1001

KEYB Assembly

SEMICONDUCTORS

Mark	Symbol & Description		Part No.
	IC1	Transistor array	TD62504P
	D2 – D5		SLH-56MC3H
	D1		SLH-56VC3H

SWITCHES

Mark	Symbol & Description		Part No.
	S1 – S7	Tact switch (PLAY, REJECT, STEP.R, STEP F, SCAN R, SCAN F, DISPLAY)	VSC-012

FILTERS

Mark	Symbol & Description		Part No.
	F3	Ferrite bead	ATF1003
	F1, F2	EMI filter	VTH1011

CAPACITORS

Mark	Symbol & Description		Part No.
	C1		CEAS470M25
	C2		CKPUYF223Z25

RESISTORS

Mark	Symbol & Description		Part No.
		All resistors	RD1/6PM□□□J

OTHER

Mark	Symbol & Description		Part No.
		IR sensor unit	GP1U50X

PWID Assembly

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	D101	SLH-56VC3H

RESISTOR

Mark	Symbol & Description	Part No.
	R101	RD1/6PM271J

HOUR Assembly

RESISTORS

Mark	Symbol & Description	Part No.
	All resistors	RD1/6PM□□□J

REGB Assembly (DWR1032)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC1	M5218L
	Q10, Q12	2SA933S
	Q2, Q6	2SB941
	Q13	2SC1627
	Q11	2SC1740S
	Q5	2SC3243
	Q1, Q3, Q4, Q7, Q8, Q14	2SD1267
	D9, D10	HZS10NB2
	D13, D14	HZS5.6NB2
	D2	RB-152LF-F
	D1	RBA-402
	D3	RBV-402
	D17	S2K20
	D5 – D8, D11, D12	1SS254

COIL

Mark	Symbol & Description	Part No.
	L1 Choke coil	VTT-070

CAPACITORS

Mark	Symbol & Description	Part No.
	C27, C29	CEAS100M50
	C18 – C20, C24, C25	CEAS101M10
	C13, C21	CEAS103M10
	C5, C8, C10	CEAS221M25
	C26	CEAS4R7M50
	C11	CEAS470M25
	C1, C2, C4, C7	CEAS472M25
	C14	CEAS682M10
	C32	CEHAQ331M6R3
	C17	CEHAQ470M10
	C30	CKCYB332K50
	C33 – C36	CKCYF103Z50
	C28	CKPUYB471K50
	C6, C9, C15, C16	CKPUYF223Z25
	C31	CQMA102K50

RESISTORS

Mark	Symbol & Description	Part No.
	R24 (3W 0.47Ω)	DCN1013
	R8, R9, R30	RD1//2PMF□□□J
	R23, R25 – R27	RN1/6PQ□□□□F
	R22 (1W 2.7Ω)	VCN-100
	Other resistors	RD1/6PM□□□J

LSFB Assembly

SWITCH

Mark	Symbol & Description	Part No.
⚠	S101 Power switch	VSA-011

FILTER

Mark	Symbol & Description	Part No.
⚠	L101 Line filter	VTL-157

CAPACITORS

Mark	Symbol & Description	Part No.
⚠	C101 – C104 Ceramic capacitor (0.01μF/AC400V)	RCG-009

DEGE Assembly (DWV1033)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC4	HD440072
	IC1, IC3	HD74HC221P
	IC2	HD74HC74P
	IC403	M5233P
	IC402	NJM4558S
	IC5	NJU4053BD
	IC401	PA0034A
	IC202	PA3018
	IC201	PA5010
	IC204	PA9003
	IC203	PM0001
	IC6	TC4053BP
	Q3, Q4, Q404, Q412	UN4212
	Q1, Q5, Q8 – Q10, Q201, Q202, Q219, Q220, Q226, Q228, Q405, Q411, Q413	2SA933S
	Q2, Q6, Q203 – Q218, Q224, Q225, Q227, Q229 – Q331, Q401, Q402, Q406 – Q410	2SC1740S

Mark	Symbol & Description	Part No.
	Q11	2SC3581
	Q12	2SK161
	Q403	2SK184
	D6	HZS7B1
	D1, D2, D5, D201, D401 – D411, D414	1SS254
	D3, D4, D7	1SV68

SWITCH AND RELAY

Mark	Symbol & Description		Part No.
	S1	Lever switch	VSK-005
	RY401	Relay	VSR-005

COILS AND FILTERS

Mark	Symbol & Description		Part No.
	L205	Axial inductor	LAU100J
	L2, L202, L203, L210	Axial inductor	LAU120J
	L209	Axial inductor	LAU121J
	L204	Axial inductor	LAU150J
	L206	Axial inductor	LAU220J
	L215	Axial inductor	LAU330J
	L201, L218	Axial inductor	LAU390J
	L220	Axial inductor	LAU470J
	L216	Axial inductor	LAU560J
	L219	Axial inductor	LAU680J
	L1	Axial inductor	LAU820J
	L213, L214, L3, L4	Radial inductor	LRA221J
	L5	Radial inductor	LRA222K
	L207, L208	Radial inductor	LRA391K
	L211	Radial inductor	LRA561K
	F201	1.75MHz L.P.F.	VTF1021
	F401	Audio B.P.F	VTF1025
	F402	2.3MHz B.P.F	VTF1026
	F403	2.8MHz B.P.F	VTF1003
	F3, F4	3 terminal filter	VTH1001
	F1, F2, F5	Ferrite bead	DTF1003

CAPACITORS

Mark	Symbol & Description	Part No.
	C23, C36	CCCCH040D50
	C20, C14	CCCCH060D50
	C213	CCCCH080D50
	C241 C335	CCCCH080D50
	C44, C303, C318	CCCCH101J50
	C215, C338, C317	CCCCH120J50
	C243	CCCCH121J50
	C234, C239, C289	CCCCH150J50
	C232, C233, C247, C274	CCCCH180J50
	C273	CCCCH220J50
	C339, C337	CCCCH270J50
	C214	CCCCH330J50
	C204, C336, C26	CCCCH390J50
	C256, C301, C326	CCCCH430J50

Mark	Symbol & Description	Part No.
	C286, C288, C245	CCCCH470J50
	C306, C422, C423	CCCCH560J50
	C305	CCCCH620J50
	C33, C253	CCCCH680J50
	C209, C210	CCCCH820J50
	C307	CCCCH910J50
	C275	CCCSL121J50
	C19, C34, C295, C296	CCCSL151J50
	C261, C262, C279	CCCSL181J50
	C290	CCCSL241J50
	C24, C211, C419	CCCSL271J50
	C418	CCCSL301J50
	C246, C328	CCCSL331J50
	C212	CCCSL391J50
	C466	CCCSL681J50
	C25	CCCUJ270J50
	C441	CEANLR47K50
	C444	CEANP2R2M50
	C263, C424, C425, C430, C431	CEANP220M10
	C260	CEANP3R3M50
	C271, C276, C442	CEANP470M10
	C229, C327	CEASR47M50
	C201, C329, C443, C465	CEAS010M50
	C7, C30, C219, C299, C308, C440, C449, C452, C453	CEAS100M50
	C320, C322, C332, C333, C414 – C417, C436, C437	CEAS221M6R3
	C13, C40, C43, C39, C408, C409	CEAS331M16
	C1, C2, C38, C42	CEAS331M6R3
	C17, C222, C285, C439, C458, C459	CEAS4R7M50
	C3, C11, C12, C16, C29, C31, C41, C206, C208, C224, C226, C228, C231, C236, C249, C252, C255, C257, C265, C270, C272, C281, C282 C284, C298, C300, C310, C314, C316, C325, C330, C331, C403, C404, C454, C455, C468	CEAS470M16
	C467	CFTXA224J50
	C203, C216, C293, C438	CFTXA104J50
	C292, C35, C334	CFTXA473J50
	C22, C242, C244, C446, C447	CKPUYB102K50
	C217, C218, C237, C238, C240, C250, C267, C268, C401, C402	CKPUYF103Z25
	C4, C10, C15, C28, C32, C37, C202, C205, C207, C223, C225, C227, C230, C235, C248, C251, C254, C258, C259 C264, C266, C269, C280, C283, C291, C294, C297, C302, C304, C309, C313, C315, C319, C321, C340, C341, C405, C406, C410 – C413, C434, C435, C456, C457, C469, C470	CKPUYF223Z25
	C5, C6, C9	CQMA102J50
	C278	CQMA103J50
	C420, C421	CQMA152J50
	C18	CQMA182J50
	C221	CQMA183J50

Mark	Symbol & Description		Part No.
	C448		CQMA222J50
	C277		CQMA272J50
	C21, C27		CQMA392J50
	C432, C433		CQMA393J50
	C426 – C429		CQMA472J50
	C287, C463		CQMA683J50
	C220		CQSA821J50
	VC1, VC2	Ceramic trimmer (20P)	VCM-008

RESISTORS

Mark	Symbol & Description		Part No.
	VR202	Semi-fixed (1kΩ)	VRTB6VS102
	VR201, VR204, VR401	Semi-fixed (1kΩ)	VRTG6HS102
	VR203	Semi-fixed (4.7kΩ)	VRTG6HS472
	R219 – R221, R223, R225, R234, R248, R249, R251, R252, R483, R485		RN1/6PQ□□□□F
		Other resistors	RD1/6PM□□□J

OTHERS

Mark	Symbol & Description		Part No.
	JA3	Pin jack (2Pin)	DKB1010
	JA1, JA2	Pin jack (2Pin)	DKB1011
	X1	Crystal resonator	VSS1005
	DL201	220nsec Delay line	VTF-063
		BNC assembly	DKN1018
		BNC holder	DNF1152

DADB Assembly (DWV1034)

Mark	Symbol & Description	Part No.
	IC110	BU4053B
	IC104	CXD1130Q
	IC105	CXK5816M-12L
	IC107	LC7881-C
	IC108, IC109	M5218P
	IC102, IC103	NJM082D
	IC111	NJM78L05A
	IC112	NJM79L05A
	IC106	PDE024
	IC101	TC40H004P
	Q203	2SA933S
	Q201, Q202	2SC1740S
	D102	FC54M
	D101	KV1225YBR
	D103, D104, D201, D202	1SS254

COILS

Mark	Symbol & Description		Part No.
	VL101	Variable coil (3.8μH)	VTL-275
	L101	Coil (4.7μH)	VTL1003

CAPACITORS

Mark	Symbol & Description	Part No.
	C201. C203, C204	CCCCH220J50
	C118	CCCCH560J50
	C107	CCCSL331J50
	C119	CCCSL391J50
	C104	CCCUJ221J50
	C103, C120, C202	CCCUJ330J50
	C113	CEANP2R2M50
	C216, C226	CEANP220M16
	C110	CEAS010M50
	C108. C109, C116, C117, C122	CEAS100M50
	C121, C125, C127, C205	CEAS101M10
	C211, C221	CEAS220M25
	C105, C206, C209, C210, C217 – C220, C227 – C230	CEAS470M16
	C112	CFTXA104J50
	C115	CFTXA474J50
	C212, C222	CFTXA683J50
	C101, C126, C128	CGCYX473M25
	C214, C224	CKCYB561K50
	C215, C225	CKCYB681K50
	C102, C207, C208	CKCYF103Z50
	C111, C213, C223	CQMA103J50
	C231	CQMA104J50
	C106	CQMA223J50
	C114	CQMA822J50

RESISTORS

Mark	Symbol & Description		Part No.
	VR101	Semi-fixed (22kΩ)	VRTB6VS223
	R114, R115, R118, R120, R127, R128, R138		RN1/6PQ□□□□F
		Other resistors	RD1/6PM□□□J

OTHER

Mark	Symbol & Description	Part No.
	X1 Crystal resonator (16MHz)	VSS1004

DTMC Assembly (DWV1035)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC2	HA19211NT
	IC15	HA19510
	IC9 – IC12	MN4700
	IC8	MN4760S
	IC4, IC6	NJM082D
	IC1	PA5012
	IC3	PDB005
	IC14	PDB006
	IC13	SN74LS32N
	IC7	TC74HCU04AP
	Q18	UN4112
	Q19, Q20, Q23	UN4212
	Q2, Q10, Q16, Q17, Q32	2SA933S
	Q1, Q3, Q4, Q6 – Q9, Q12 – Q14, Q22, Q24, Q26 – Q28, Q33, Q34, Q36, Q38 – Q40	2SC1740S
	Q29, Q30	2SK30ATM
	D8	SVC321SP
	D1 – D6, D9	1SS254
	D7	1SV68

COILS

Mark	Symbol & Description		Part No.
	L2, L6	Axial inductor	LAU100J
	L12	Axial inductor	LAU101J
	L3, L9	Axial inductor	LAU150J
	L8	Axial inductor	LAU180J
	L7	Axial inductor	LAU270J
	L5	Axial inductor	LAU3R9J
	L1	Axial inductor	LAU470J
	L4	Radial inductor	LRA101J
	L11	Radial inductor	LRA101K
	L10	Radial inductor	LRA222K

CAPACITORS

Mark	Symbol & Description	Part No.
	C98	CCCCH080D50
	C68	CCCCH100D50
	C63	CCCSL101J50
	C100	CCCSL180J50
	C99	CCCSL820J50
	C74	CCCCH151J50
	C6, C7	CCPUCH100J50
	C9	CCPUCH160J50
	C65	CCPUCH200J50
	C22, C94	CCPUSL220J50
	C38	CCPUSL330J50
	C4, C102	CCPUSL390J50
	C97	CCPUSL470J50
	C8, C10, C78	CCPUSL680J50
	C85	CEANPR47M50
	C3	CEANP010M50
	C87	CEANP100M16
	C57	CEANP220M10
	C103	CEANP470M10
	C36, C93, C48	CEAS010M50
	C12 – C14, C46, C47	CEAS100M50
	C30	CEASR47M50
	C44	CEAS3R3M50
	C1, C91, C106, C84	CEAS331M6R3
	C17, C24, C28, C32, C49, C50, C52, C53, C56, C58, C64, C69, C83, C88, C95, C109	CEAS470M10
	C29	CKCYB103K50
	C2, C108	CKCYF103Z50
	C71, C79, C81, C104	CKPUYB101K50
	C70	CKDYF103Z50
	C80	CKPUYB102K50
	C35	CKPUYB151K50
	C39	CKPUYX222M16
	C37, C73	CKPUYB331K50
	C77	CKPUYB681K50
	C41	CKPUYB820K50
	C16, C18 – C20, C23, C33, C34, C40, C43, C51, C54, C59, C61, C66, C82, C86, C90, C92, C96, C107	CKPUYY103N16
	C26	CQMA103J50
	C60	CQMA104J50
	C76	CQMA122J50
	C62	CQMA153J50
	C72	CQMA332J50
	C75	CQMA682J50
	C42	CQMA472J50
	VC1 Ceramic trimmer (20pF)	VCM-008

RESISTORS

Mark	Symbol & Description		Part No.
	VR6	Semi-fixed (1kΩ)	VRTB6VS102
	VR1, VR2, VR4	Semi-fixed (10kΩ)	VRTB6VS103
	VR3	Semi-fixed (22kΩ)	VRTB6VS223
	VR7	Semi-fixed (470Ω)	VRTB6VS471
		Other resistors	RD1/6PM☐☐☐J

OTHERS

Mark	Symbol & Description		Part No.
	X1	Crystal resonator	VSS1021
		Thro type capacitors assembly	DXX1248

BLDB Assembly (DWR1031)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC301	TA8413P
	Q301 Transistor array	SLA4020
	Q302 Transistor array	SLA4030
	Q303 – Q305	2SA1048
	D301 – D303	S2V10-4001

CAPACITORS

Mark	Symbol & Description	Part No.
	C304	CEAS4R7M50
	C305	CKPUYF103Z25
	C301 – C303 (33μF/50V)	VCH1034

RESISTORS

Mark	Symbol & Description	Part No.
	All resistors	RD1/6PM□□□J

PREB Assembly (DWV1032)

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC1	IR3C02A
	IC2 – IC5, IC10, IC14	NJM082D
	IC6 – IC9	NJM311D
	IC11	NJM4556DE
	IC12, IC13	NJM4558D
	IC15	TC4052BP
	Q14, Q16, Q18, Q19	UN4112
	Q3, Q21, Q22	UN4212
	Q5, Q7, Q9	2SB1185-F8
	Q10	2SB949
	Q1, Q2	2SC1740S
	Q11	2SD1275
	Q4, Q6, Q8	2SD1762-F8
	Q15, Q17	2SD1859
	Q12, Q13, Q20, Q23, Q24	2SK184
	D11, D12	HZS10EB3
	D13	HZ5B2
	D19	HZS8.2EB2
	D14, D15	1SR139-400
	D1 – D10, D16 – D18	1SS254

CAPACITORS

Mark	Symbol & Description	Part No.
	C18, C19	CCCCH680J50
	C39	CFTXA224J50
	C21	CEALNP4R7M16
	C5, C7	CEAL010M50
	C11	CEAL101M6R3
	C23, C25, C32, C35, C51, C54, C79, C81	CEAL220M16
	C2, C4, C8, C10, C13, C75, C77	CEAL220M6R3
	C44, C46, C56, C58, C62, C64, C66, C67, C69 – C72, C84 C86	CEAL330M25
	C59	CEANP470M16
	C90, C91	CKPUYB102K50
	C87, C88, C74	CKPUYB221K50
	C73	CKPUYB561K50
	C61, C68	CKPUYB681K50
	C1, C3, C6, C9, C12, C14, C16, C17, C22, C24, C27 – C29, C33, C34, C37, C38, C41 – C43, C45, C52, C53, C55, C57, C63, C65, C76, C78, C80, C82, C83, C85	CKPUYF223Z25
	C48	CQMA102J50
	C26	CQMA103J50
	C30, C89	CQMA152J50
	C20	CQMA153J50
	C36	CQMA222J50
	C40	CQMA472J50
	C50	CQMA223J50
	C47	CQMA393J50
	C49	CQMA563J50
	C31	CQMA683J50

RESISTORS

Mark	Symbol & Description	Part No.
	VR6 Semi-fixed (100kΩ)	VRTB6VS104
	VR7 Semi-fixed (1MΩ)	VRTB6VS105
	VR1 Semi-fixed (2.2kΩ)	VRTB6VS222
	VR4 Semi-fixed (15kΩ)	VRTB6VS153
	VR3 Semi-fixed (47kΩ)	VRTB6VS473
	R126	RS1PMF4R7J
	R134	RD1/2PMF2R2J
	R108, R114, R122 (47Ω 1/6W) Fuse resistor	DCN1003
	R116, R117, R124, R125 (2.2Ω1/4W) Fuse resistor	DCN1014
	R127	RD1/2PMF2R7J
	Other resistors	RD1/6PM□□□J

OTHER

Mark	Symbol & Description	Part No.
	CN10 30 pin connector	VKN1071

POSS Assembly

SEMICONDUCTOR

Mark	Symbol & Description	Part No.
	IC501 Photo reflector	GP1A30R

CAPACITOR

Mark	Symbol & Description	Part No.
	C501	CKPUYF223Z25

RESISTOR

Mark	Symbol & Description	Part No.
	R501	RD1/6PM121J

HEAD Assembly

COIL

Mark	Symbol & Description	Part No.
	L1	VTL1007

CAPACITORS

Mark	Symbol & Description	Part No.
	C1	CKSQYF473Z50
	C2	CKSYF105Z16

RESISTOR

Mark	Symbol & Description	Part No.
	VR1 Semi-fixed (10kΩ)	VCP-142

LMCB Assembly

SEMICONDUCTORS

Mark	Symbol & Description	Part No.
	IC1	TA7291P
	D1	HZS9B3

CAPACITORS

Mark	Symbol & Description	Part No.
	C1	CGDYX473M25
	C3	CEAS100M50

RESISTORS

Mark	Symbol & Description	Part No.
	All resistors	RD1/4VM□□□J

Thru Type Capacitors Assembly (DXX1248)

CAPACITORS

Mark	Symbol & Description	Part No.
	C501 — C531 Thro type capacitor (100pF)	VCG1006
	C532 — C536 Thro type capacitor (1000pF)	VCG1007

7. DISASSEMBLY

7.1 HOW TO REPLACE THE PICK-UP ASSEMBLY (Fig. 7-1 ~ 4)

① Remove the six screws Ⓐ to remove the bottom plate.
② Remove the flexible board (HEAD assembly) of the pickup assembly from the PREB assembly.

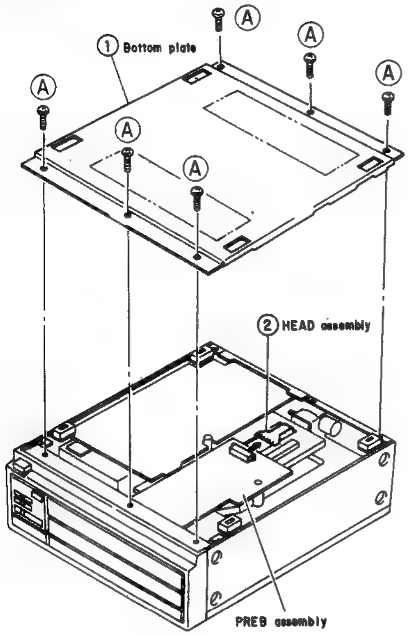


Fig. 7-1

③ Remove the four screws Ⓑ to remove the top plate.
④ Switch the power ON and press the EJECT button to open the disc tray.
⑤ Remove the two screws Ⓒ of the DSCO assembly and the three screws Ⓓ of the sub rear panel A, then stand the DSCO assembly up at a right angle 90° while extending the (wire) harness.

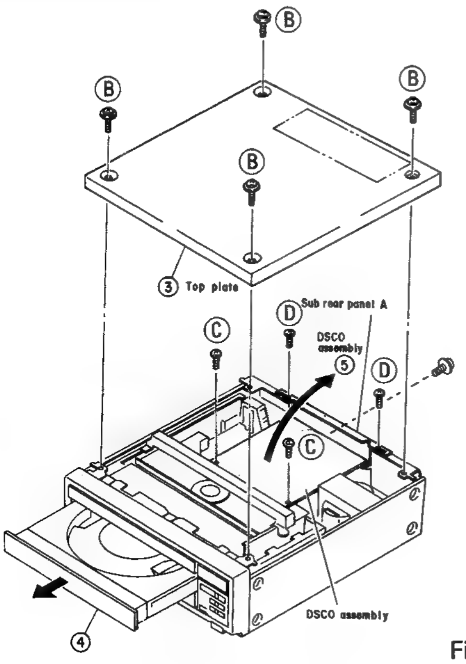


Fig. 7-2

⑥ At this time, after standing up the DSCO assembly at a right angle 90° using the section A as a support, pull the DSCO assembly in the direction of the arrow to fix it.

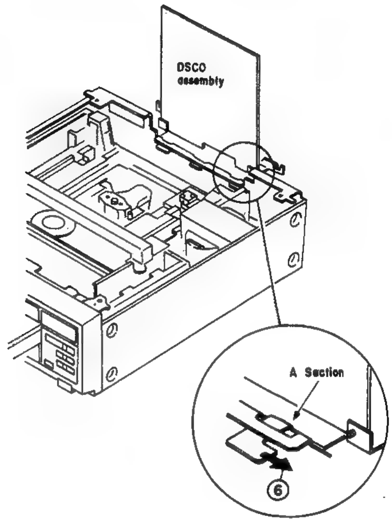


Fig. 7-3

⑦ Remove the two D-coils and S-coils connected to the pickup flexible board by unsoldering them.
(Subsequent operations should be performed with the power switched OFF as the slider is locked and the pick-up position fixed.)
⑧ Remove the screw Ⓔ of the flexible board mounted on the slider.
⑨ Pull out the flexible board inserted into the POSS assembly.
⑩ Remove the screw Ⓕ of the pickup assembly secured to the pick-up holder, and now the pickup assembly can be removed by lifting it up.

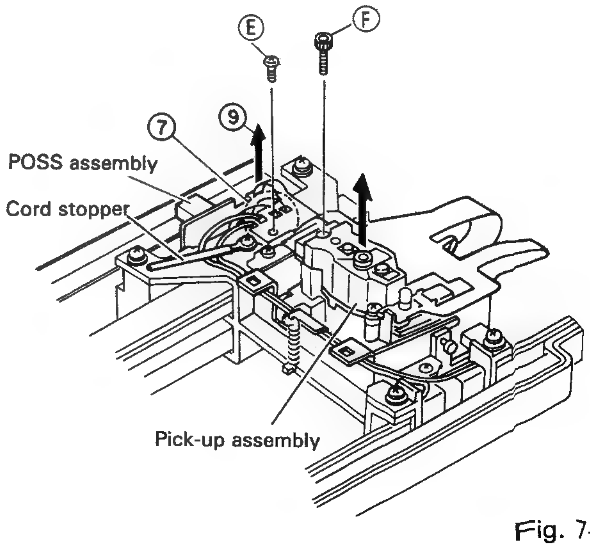


Fig. 7-4

7.2 HOW TO INSTALL THE PICK-UP ASSEMBLY (Fig. 7-5)

When installing a new pick-up, perform the following procedure so that the flexible board (HEAD assembly) can be inserted easily into the POSS assembly.

① Remove the position sensor block (two reinforcement plates and the slit plate) from the tilt base by removing the three screws Ⓐ.

② Remove the POSS assembly from the shaft holder by removing the two screws Ⓑ.

③ Mount the flexible board to the POSS assembly. After this, reassemble by reversing the disassembly procedure.

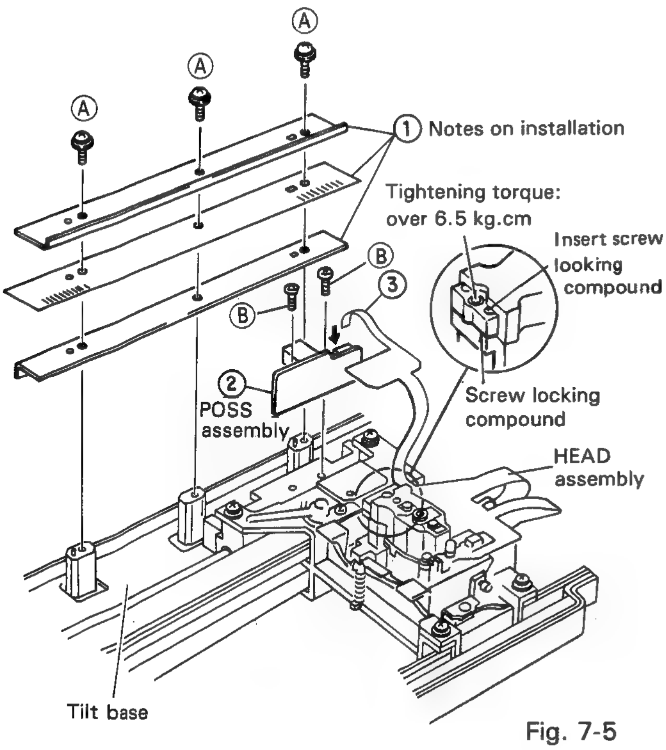


Fig. 7-5

7.3 CLEANING THE LENS

As shown in Fig. 7-6, clean the lens using the lens cleaning jig.

• Conditions for cleaning

'87 Pick-up

1. Use lens cleaning fluid GEM1004 and cleaning paper GED-008.
2. To clean, wipe the lens surface by turning it with a pressure of 10 — 20 g, about 10 times at a time.
3. So that the actuator is not distorted, be sure to use lens cleaning jig GGF-194.

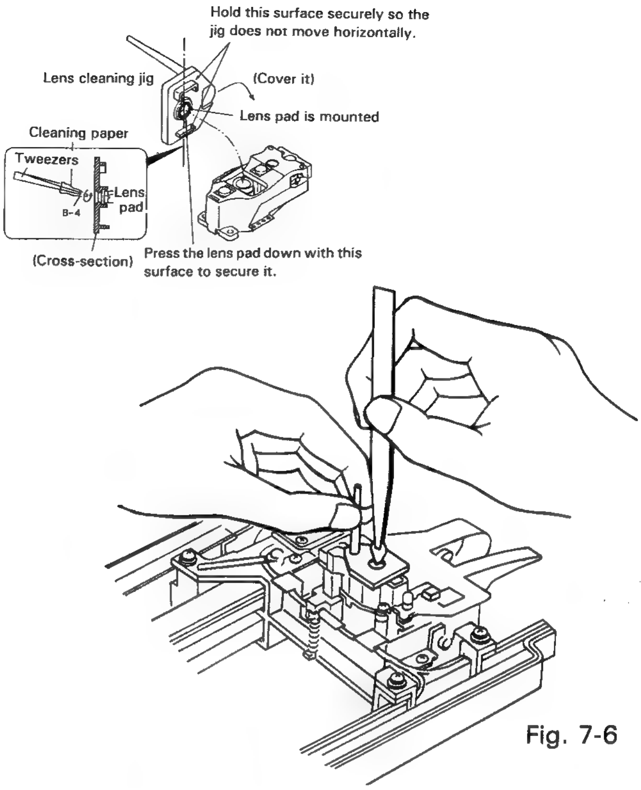


Fig. 7-6

7.4 HOW TO REMOVE THE DISC TABLE (Fig. 7-7)

Perform the steps ① — ⑥ in the procedures of "7.1 How to Replace the Pick-up Assembly".

① Slightly push the disc table inward and remove the two screws Ⓐ to remove the two stop plates.

② Pull out the plastic rivet upward, and remove the screw Ⓑ to remove the switch metal assembly.

③ Pull out the disc table slowly to remove it.

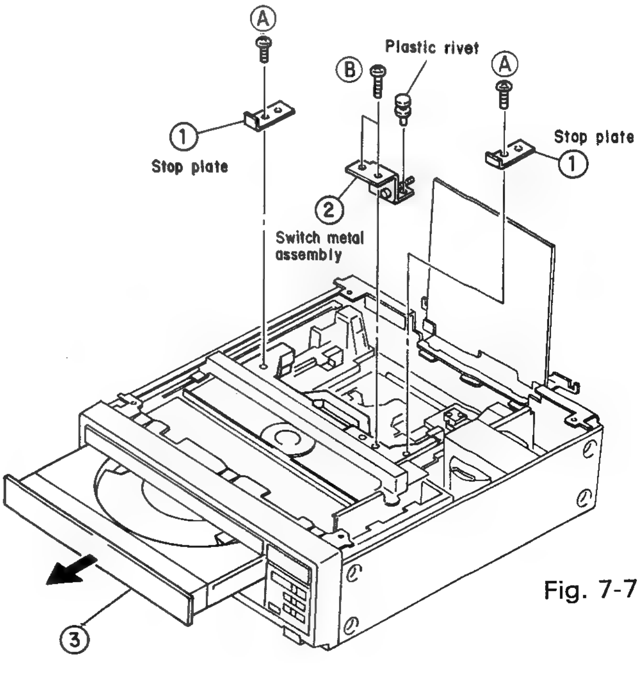


Fig. 7-7

7.5 HOW TO CLAMP THE DISC WHEN THE DISC TABLE IS REMOVED (Fig. 7-8)

① Insert the disc from the rear and place it on the turntable.

Note: When inserting the disc, be careful not to get grease on the recorded surface of the disc.

② While spreading the (L) and (R) lock levers outward, press them toward the rear panel to lower the clamp so it clamps the disc.
Check that the disc has been clamped correctly, by rotating the clamper with your hand.

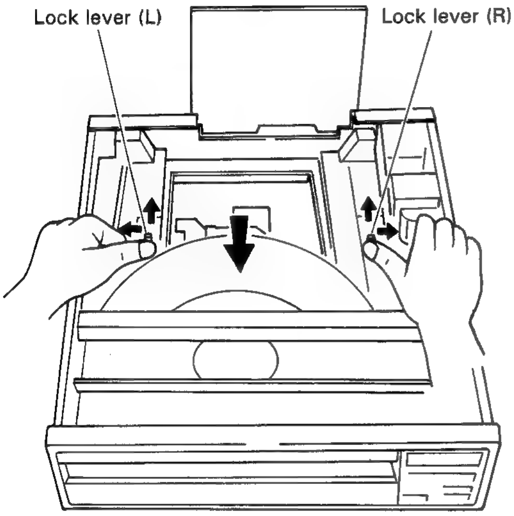


Fig. 7-8

7.6 HOW TO PLAY THE DISC WHEN THE DISC TABLE IS REMOVED (Fig. 7-9)

While pressing the clamp switch, switch the power ON, then press the PLAY button.

After pressing the PLAY button, release the clamp switch.

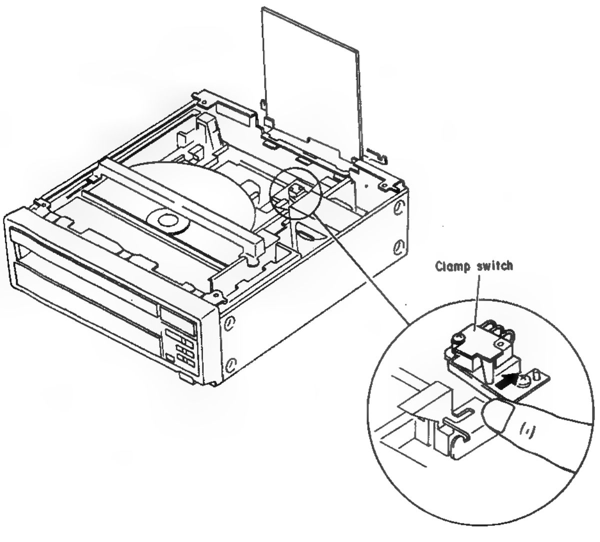


Fig. 7-9

7.7 HOW TO INSTALL THE DISC TABLE (Fig. 7-10)

① Remove the four screws Ⓐ of the DADB assembly to lift up the DADB assembly.

② Match the non-toothed section of the inside gear with the notch of the disc table gear to engage them, and insert the disc table.

③ Mount the metal switch assembly and the two stop plates which were removed in Fig. 7-7.

④ Install the DADB assembly which was removed in step ①.

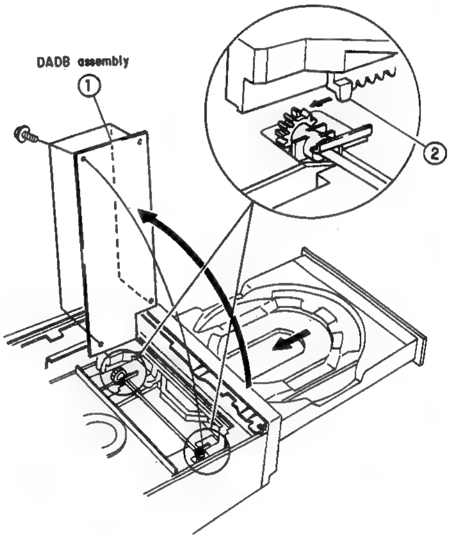


Fig. 7-10

7.8 HOW TO RELEASE THE AUTO LOCK MECHANISM (Fig. 7-11)

① Remove the four screws Ⓐ to remove the side panel (L).

② Press the lock arm in the direction of the arrow to release the auto lock mechanism.

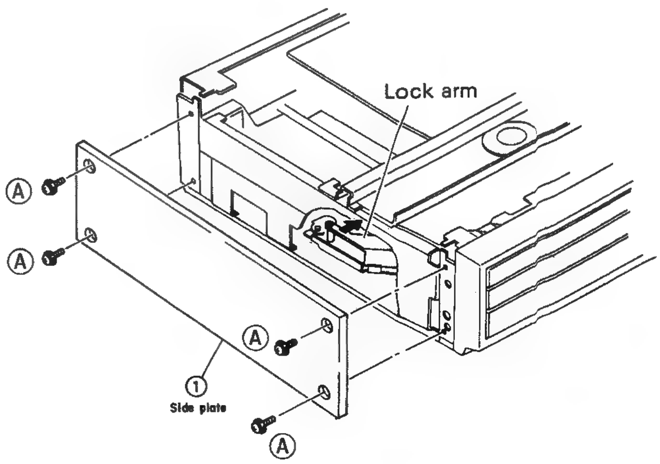
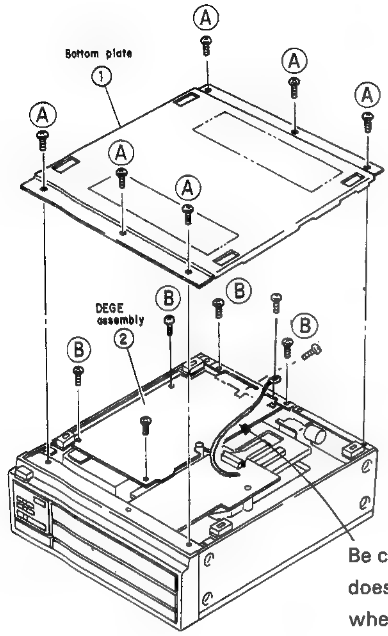


Fig. 7-11

7.9 HOW TO REMOVE THE MECHANISM ASSEMBLY (Fig. 7-12, 13)

① Remove the six screws Ⓐ to remove the bottom plate.
② Remove the seven screws Ⓑ to remove the DEGE assembly.



Be careful the styling does not touch the tilt base when installing.

Fig. 7-12

③ Remove the tilt spring mounted at the rear of the tilt base on the mechanism assembly.
④ Remove the three screws Ⓒ, and remove the mechanism assembly from the tilt motor assembly, by pulling it towards the front in the direction of an arrow.

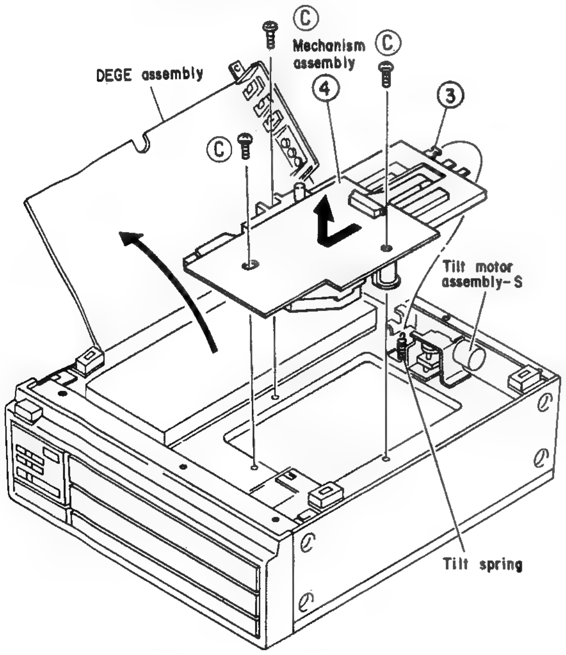


Fig. 7-13

7.10 HOW TO REMOVE THE SPINDLE MOTOR ASSEMBLY-S AND BLDB ASSEMBLY (Fig. 7-14)

① After removing the mechanism assembly, remove the two screws Ⓐ holding the BLDB assembly and the screw Ⓑ holding the spindle motor assembly-S. Now remove the BLDB assembly and spindle motor assembly-S from the mechanism chassis.
② Take out the BLDB assembly from the Spindle motor assembly-S.

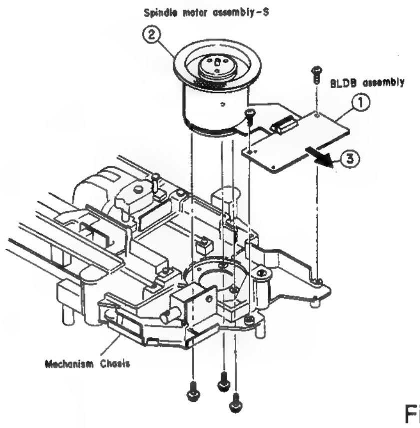


Fig. 7-14

7.11 HOW TO REMOVE THE TILT MOTOR (Fig. 7-15)

① Remove the six screws to remove the bottom plate. (See Fig. 7 — 12)
② Remove the two screws Ⓐ to remove the tilt gear assembly from the chassis base.
At this time, since the tilt base of the mechanism assembly is pulled by a spring, be careful not to stretch the tilt spring.
③ Remove the two screws Ⓑ of the tilt gear assembly to remove the tilt motor assembly-S.

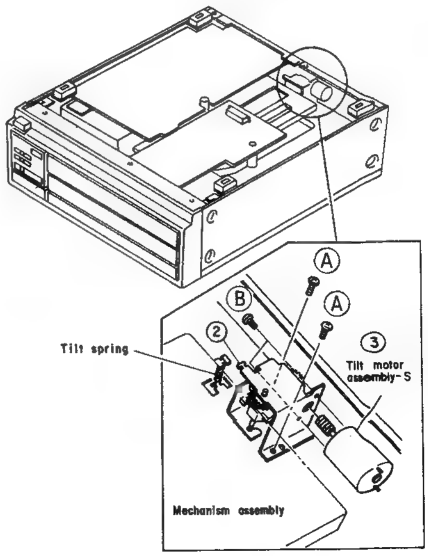


Fig. 7-15

8. SERVICE MODE

The service mode is provided for the adjustment of the player; do not use this mode apart for adjustment. And in the service mode, since no backup processing is provided, operations will not stop automatically even if a malfunction occurs. Because of this, be particularly careful as the player could be damaged.

8.1. HOW TO ENTER THE SERVICE MODE

To enter the service mode, perform the following:

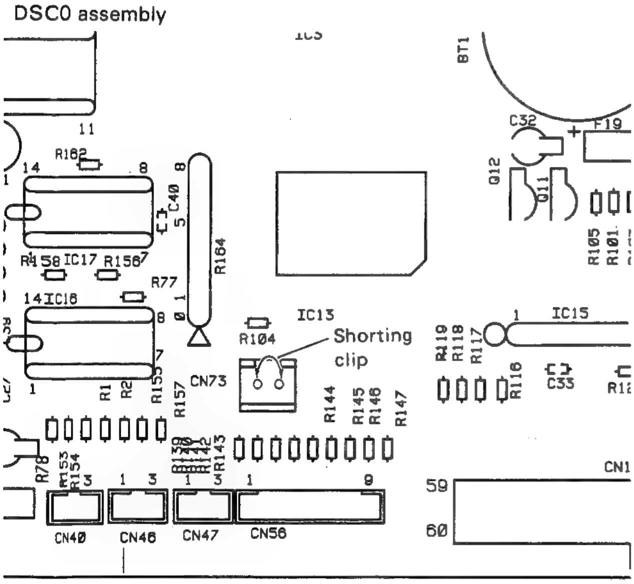
(1) To enter the test mode:

As the service mode is part of test mode, you must first enter the test mode.

a. To use the test pin:

When the test pin (CN73) on the DSCO assembly is short-circuited, the player will enter the test mode and the menu screen appears.

DSCO assembly



b. To use the function switch:

Using the function switch setup mode, set the TEST MODE to ON. After this, when the power is turned ON, the player enters the Diagnosis mode of test mode. When the Display key is pressed twice, the menu screen will appear.

(2) To enter the service mode

When the operations in (1) are performed, the menu screen appears. In this condition, you can enter the service mode.

Press the Step Forward key twice; the "Service Mode" indication will be marked. In this condition, press the Step Reverse key to enter the service mode.

8.2. HOW TO OPERATE THE PLAYER IN THE SERVICE MODE

(1) Play key:

In the service mode, the Play key is used to control the laser, focus and on/off switching of the spindle motor.

When the Play key is pressed with all the switches set to OFF, the focus is turned ON. When the Play key is pressed with the focus locked, the spindle motor is turned ON. After this, when the Play key is pressed with the spindle locked, all the switches are turned OFF.

(2) Step keys:

The Step keys are used to control the on/off switching of the tracking.

When the Step Forward key is pressed, the tracking is turned ON, and when the Step Reverse key is pressed, the tracking is turned OFF.

(3) Multi Speed keys: (Remote control only)

Note: In the service mode, the slider lock is normally released. Use this function only when necessary.

The Multi Speed keys are used to control the locking of the slider.

When the Multi Forward key is pressed, the slider is locked. When the Multi Reverse key is pressed, the slider lock is released.

(4) Scan keys:

The Scan keys are used to control the movement of the slider.

The slider is moved toward the outer edge of the disc only when the Scan Forward key is depressed.

The slider is moved toward the inner edge of the disc only when the Scan Reverse key is depressed.

(5) Display key:

The Display key is used to control the on-screen display.

Two on-screen displays are available. One is the "How to Use Explanation Menu" which is displayed when the service mode is entered. The other is the "Chapter/Frame No. and Pickup Position Menu". Each time the Display key is pressed, the on-screen display alternates between these two menus.

(6) Open/Close key, Reject key:

These keys are used to quit the service mode.

Note: Still cannot be performed in the service mode.

8.3. HOW TO RETURN TO THE NORMAL MODE

In the service mode, when the Reject key is pressed, the menu screen for the test mode is restored. At this time, select "Exit Test Mode". In this condition, press the Step Reverse key to return to the normal mode.

9. ADJUSTMENTS

9.1 ADJUSTING JIG AND TOOLS REQUIRED FOR ADJUSTMENT

- Small flat-bladed ⊖ screwdriver (with a shaft of about 7 cm)
- Small Philips ⊕ screwdriver (with a shaft of more than 15 cm)
- Hexagonal wrench (Allen wrench) (2.00 mm)
- Low-pass filter (100 kohms + 1 μF)
- Dual-trace oscilloscope (with delay)
- Frequency counter
- LD test disc (GGV1002)
- 8-inch LDD disc (commercially available)
- Shorting clip
- Digital voltmeter

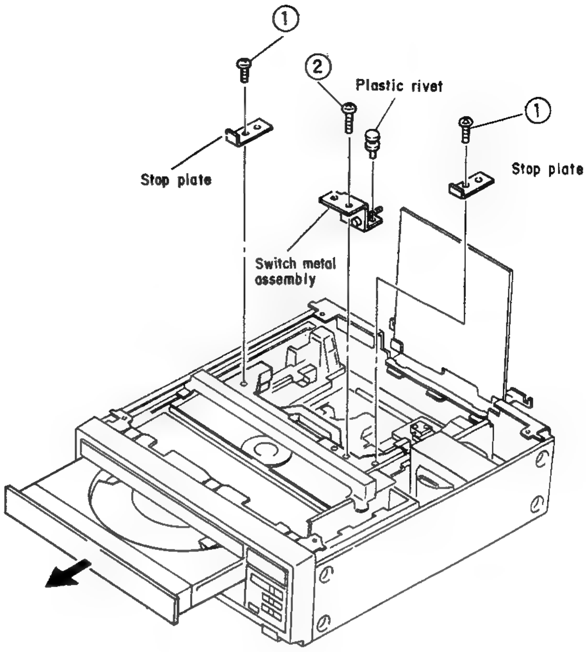


Fig. 9-1

9.2 PREPARATIONS AND PRECAUTIONS FOR ADJUSTMENT

- **Player setting**

1. Remove four screws to remove the top plate.
2. Remove six screws to remove the bottom plate.
3. Remove the four screws and unlock the two wire clamps, then raise the DSCO assembly so the PC board stands up. (Refer to "7. Disassembly".)
4. Turn the POWER switch to ON.
5. Press the OPEN/CLOSE key to slide out the tray.
6. Turn the POWER switch to OFF.
7. Push the tray with your hand to the position where the metal fittings can be removed (but do not push the tray fully to the end).
8. Remove two screws ① to remove the stop plate.
9. Remove screw ② and the plastic rivet to remove the switch metal assembly.
10. Pull out the tray toward you to remove it.
11. Turn the POWER switch to ON and immediately turn on the clamp switch on the rear panel. (Fig. 9-2)

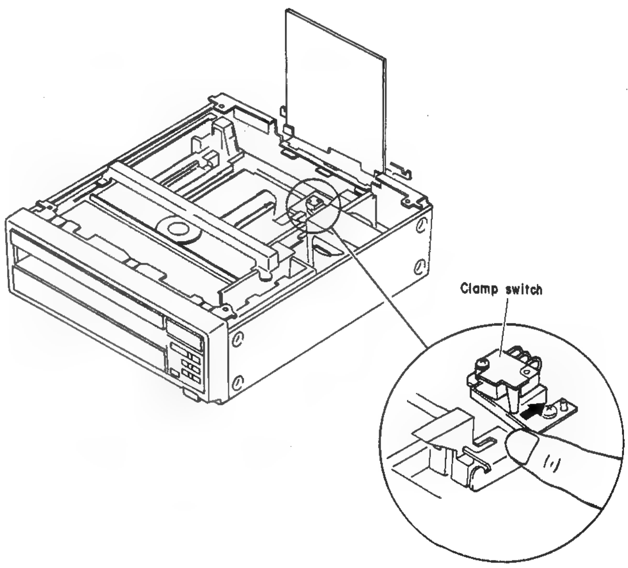


Fig. 9-2

- **How to clamp a disc**

After the disc tray is removed, insert a disc from the rear of the player. To clamp the disc, extend the lock levers located on both sides of the base toward outwards, then push them toward the rear. (Fig. 9-3)

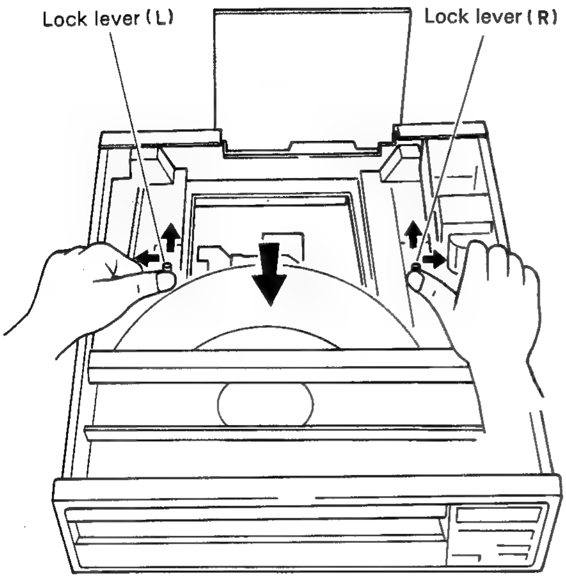


Fig. 9-3

- **How to play a disc for mechanism adjustment**

1. Set the player to the service mode. (Refer to page 87.)
2. Press the PLAY key twice, and check that the "FOCUS LOCK" indication appears on the screen.
3. Press the PLAY key again, and check that the spindle motor is turned ON and "SPINDLE LOCK" indication appears on the screen.
4. With this, the player is set to the PLAY mode, and the following can be performed if required during adjustment:
   * Press the STEP reverse key........ Tracking OPEN
   * Press the STEP forward key..... Tracking CLOSE
   However, since the still operation is not available in the service mode, release the service mode and perform adjustment in the normal mode when still operation is required for adjustment.

- **Adjustment should be performed with the player set vertically. (See Fig. 9-4.)**
  However, for 2. Grating Temporary Adjustment, Tracking Balance Adjustment, 6. Pick-up Assembly Centering Check and 7. Pick-up Assembly Centering Adjustment in the Mechanism Adjustments, the player should be set horizontally. (See Fig. 9-5.)
  If discs cannot be played with the player set vertically, first set the player horizontally and play the disc, then list the player gently to the vertical position.

- **Adjustments up to 10. RF Gain Adjustment should be performed with tilt servo OFF. (Disconnect CN28 of PREB to switch OFF the tilt servo.)**

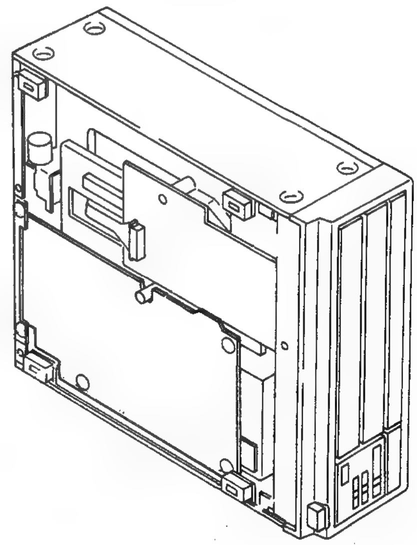


Fig. 9-4

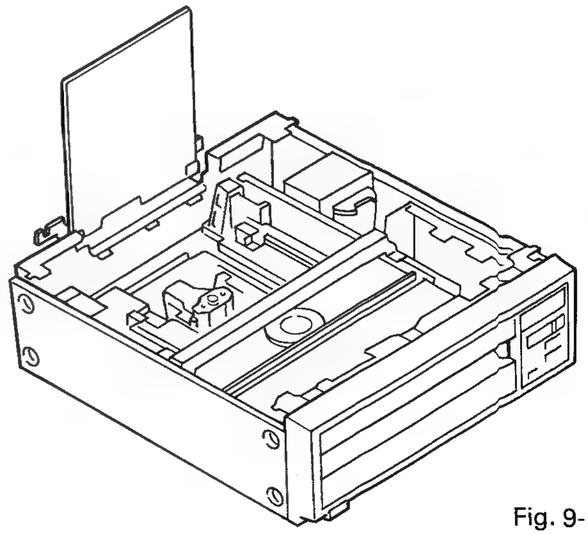


Fig. 9-5

- **How to remove the DTMC assembly (Fig. 9-6)**

1. Remove the five screws Ⓐ to remove the DTMC Assembly.

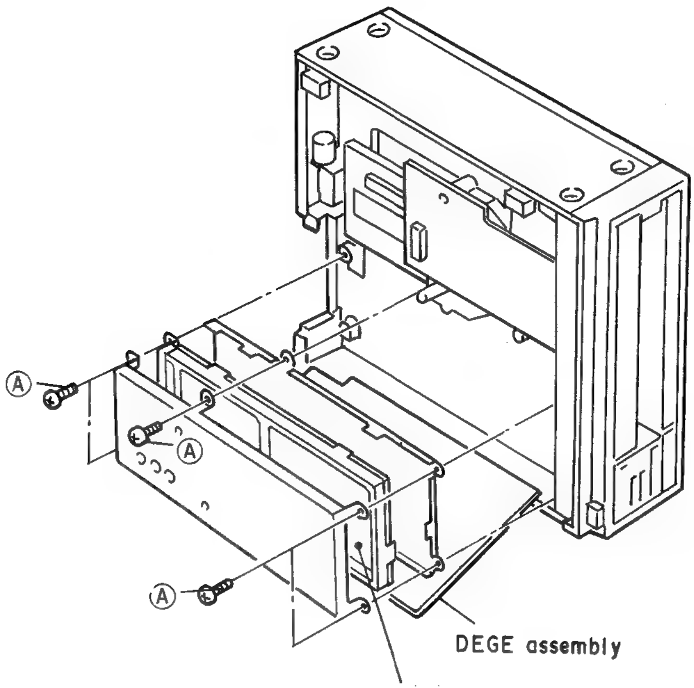


Fig. 9-6

- **The setting values for the oscilloscope for the adjustment are those when used with the 10:1 probe unless otherwise specified.**

- **How to reassemble the tray**

1. Insert the disc tray while applying the half-tooth portion of the gear to the gear of the disc tray. (Fig. 9-7.)
2. Mount the plastic rivet, switch metal assembly and the stop plates which were removed in step 8 and 9 of player setting in the previous section.

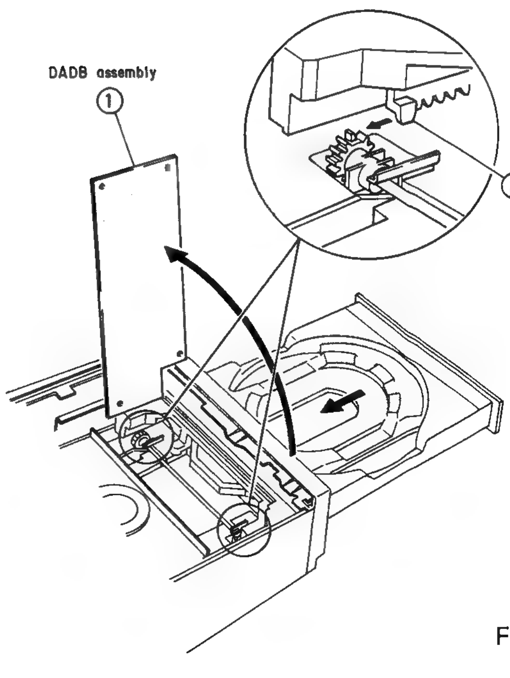


Fig. 9-7

1. TILT GAIN ADJUSTMENT

- Purpose: To adjust the gain of tilt servo according to the gain rank of the tilt sensor.
- Symptoms when incorrectly adjusted: Hunting of the tilt servo and increased crosstalk due to an increased non-sensitive range of the tilt servo.

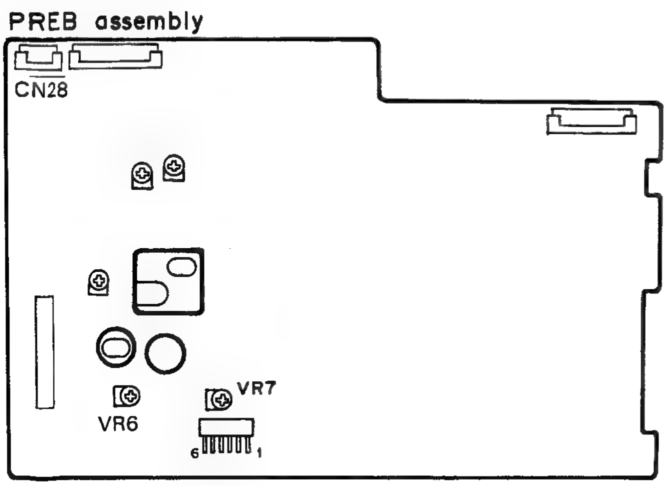
Measurement equipment & jigs	Adjusting point
• Screwdriver (flat bladed)	• VR7 in the PREB assembly

Adjusting procedure

- Check that VR6 is set to its mechanical center position, and remove the CN28 connector from the PREB assembly (to turn off the tilt servo).

1. Check the color of the dot on the flexible cable located at the side of the tilt sensor. (Fig. 1)
   There are three dot conditions: adjust VR7 on the PREB board according to the following code.
   Red dot: Turn VR7 fully clockwise.
   Blue dot: Turn VR7 fully counterclockwise.
   No dot: Set VR7 to its mechanical center position.

Adjustment diagram



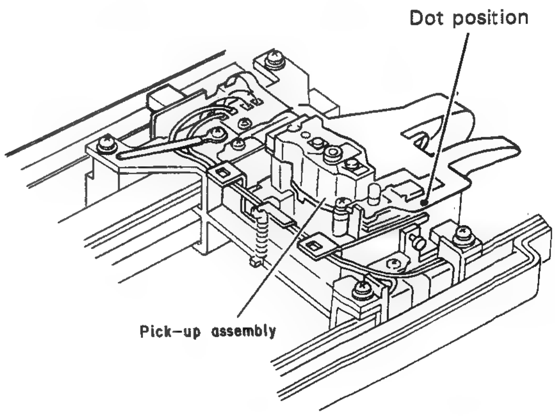


Fig. 1

2. GRATING TEMPORARY ADJUSTMENT AND TRACKING (TRKG) BALANCE ADJUSTMENT

- Purpose: Set the laser beam which is divided into three by the grating so that it is directed to the optimum position on the playback track. Set the offset voltage of the tracking servo to 0 V.
- Symptoms when incorrectly adjusted: Disc play impossible. Track jumping.

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Screwdriver (flat bladed) • Oscilloscope • Test disc: GGV1002	• Oscilloscope: In DADB assembly CH1: Between TRKG Error (TP2-2) and GND	* Service mode: • Play mode • Tracking servo loop open • Tilt servo OFF (Unplug the connector of CN28.)	• Grating adjustment screw in the pick-up assembly • VR3 in PREB assembly

Adjusting procedure

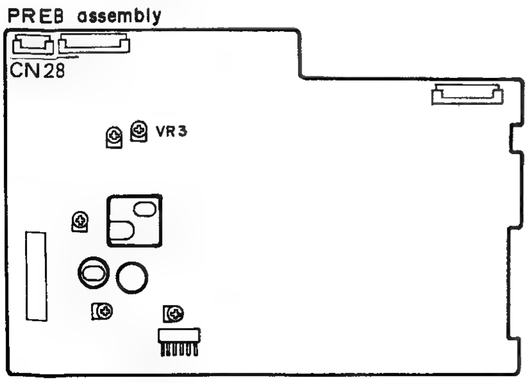
[Grating temporary adjustment]

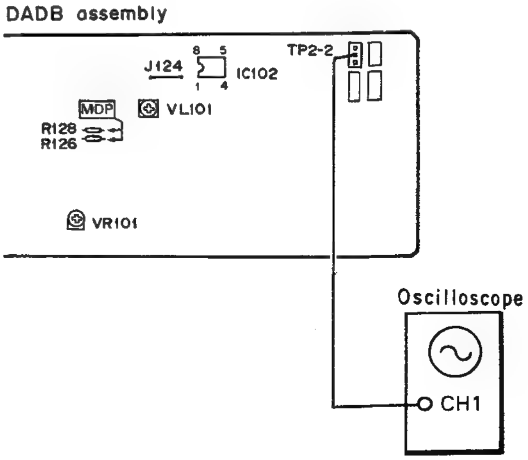
1. With the player set horizontally, play the test disc. (Refer to "How to play a disc for mechanism adjustment (Page 89).)
2. Press the DISPLAY key so that the frame number is displayed on the TV screen.
3. Using the SCAN key, move the pick-up to a position around frame #20000.
4. Open the TRKG servo loop.
5. Connect the oscilloscope to TP2-2 (TRKG error) to observe the waveforms.
6. Insert the flat bladed ⊖ screwdriver (small) into the grating adjustment hole horizontally (Fig. 2.).
   When the grating adjustment screw is turned, the tracking error waveform alternates between large and small. After the waveform amplitude becomes small, find the position where the waveform shows a smooth envelope. (Photo 1) (This status is called the "on-track" position.)
   (When adjusting the grating with the small screwdriver (flat-bladed), since the pick-up assembly tends to shift toward the inside of the disc, perform adjustment while holding it with your hand. If a remote control is available, lock the pick-up by pressing the multi-reverse key instead of holding with your hand.)
7. In this condition, when the grating adjustment screw is turned counterclockwise slowly, the amplitude of the tracking error waveform gradually becomes larger. Set to the position where the waveform amplitude becomes maximum. (Photo 2)
8. Close the Tracking servo to make sure that a picture on the screen is normal.

[TRKG (Tracking) balance adjustment]

1. Set the player to the stop mode and raise it so it is vertical, then play the test disc in the service mode.
   (Note: If the disc cannot be played in this condition, set the player horizontally and engage the service mode to start playing the disc, and then raise the left side of the player slowly, so it is vertical.)
2. Set the oscilloscope's GND point to the center of the oscilloscope screen.
3. Adjust VR3 in the PREB assembly so that the positive amplitude (A) and the negative amplitude (B) becomes equal. (Photo 2)

Adjustment diagram





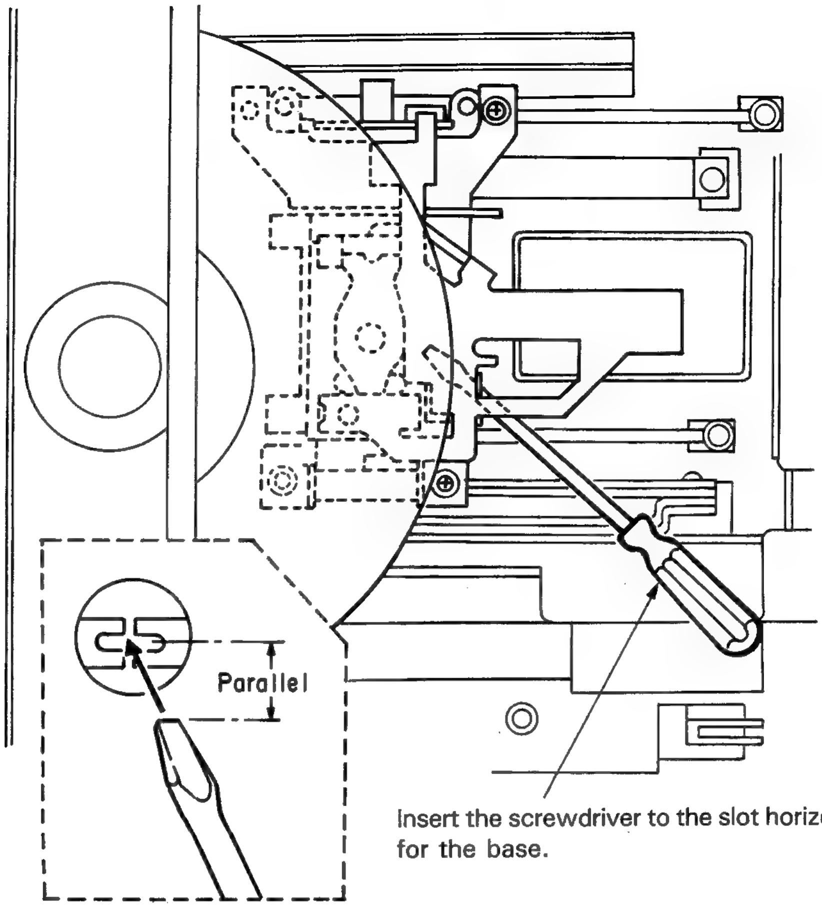


Fig. 2

Waveforms
* Oscilloscope range: DC 50 mV/div., 5 mS/div.

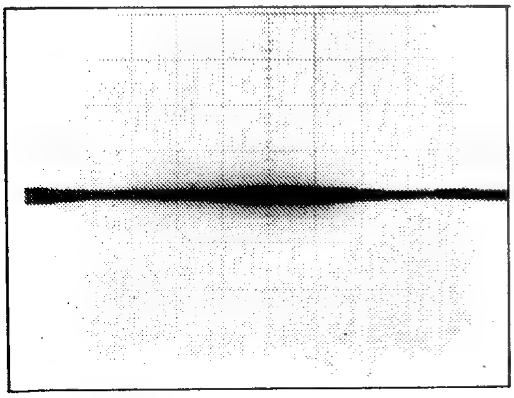


Photo 1 On-track position

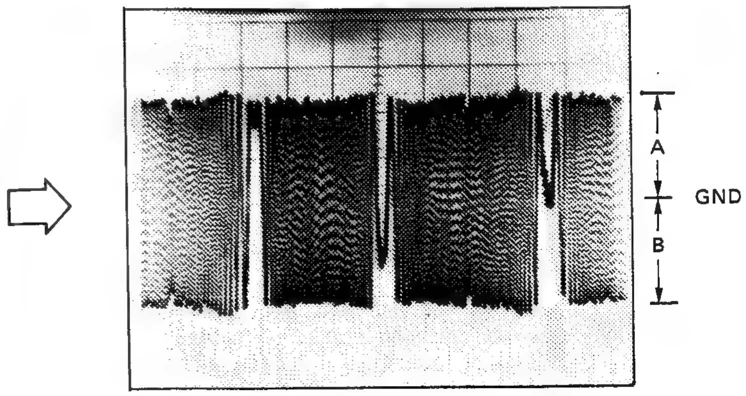


Photo 2 Maximum amplitude

3. PICK-UP HEIGHT ADJUSTMENT AND DRIVE SHAFT LEVELNESS ADJUSTMENT

- Purpose: To adjust the follow-up range of the focus servo to the optimum value.
- Symptoms when incorrectly adjusted: Lens comes contact with the disc surface, Warped discs cannot be played.

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Oscilloscope • Hexagonal wrench (2 mm) • Low-pass filter (100 kohms/1 μF) • Test disc: GGV1002	• Oscilloscope: In PREB assembly CH1: Between TP3-1 (FOCS RTN) and GND	* Service mode: • Play mode • Tracking servo loop open • Tilt servo OFF (Unplug the connector of CN28)	• Pick-up height adjustment screw in the pick-up assembly • Pinion gear of the tilt motor in the mechanism assembly

Adjusting procedure

Note: This adjustment should be performed with the unit placed horizontally.

[Pick-up assembly height adjustment]

1. Connect the oscilloscope as shown in the figure below, and play the test disc around the frame #10000.
2. Open the tracking servo loop.
3. Measure the voltage at TP3-1 (FOCS RTN) in the PREB assembly with the oscilloscope.
4. Check that the focus return voltage is 0 V ±10 mV with respect to the GND voltage. If it is out of the standard, adjust the pick-up height adjustment screw so that the voltage value comes within the standard value using the hexagonal wrench (2 mm).

[Drive shaft levelness adjustment]

5. Perform levelness adjustment by rotating the pinion gear of the tilt motor with your finger, so that the focus return voltage described above becomes the same value at the inside and outside of the disc. (Fig. 3)
   - * Frame No. 115 = V1
   - * Frame No. 10000 = V2
   - * Frame No. 22000 = V3

   V1 - V2 ≦ 20 mV

   V3 - V2 ≦ 20 mV

Adjustment diagram

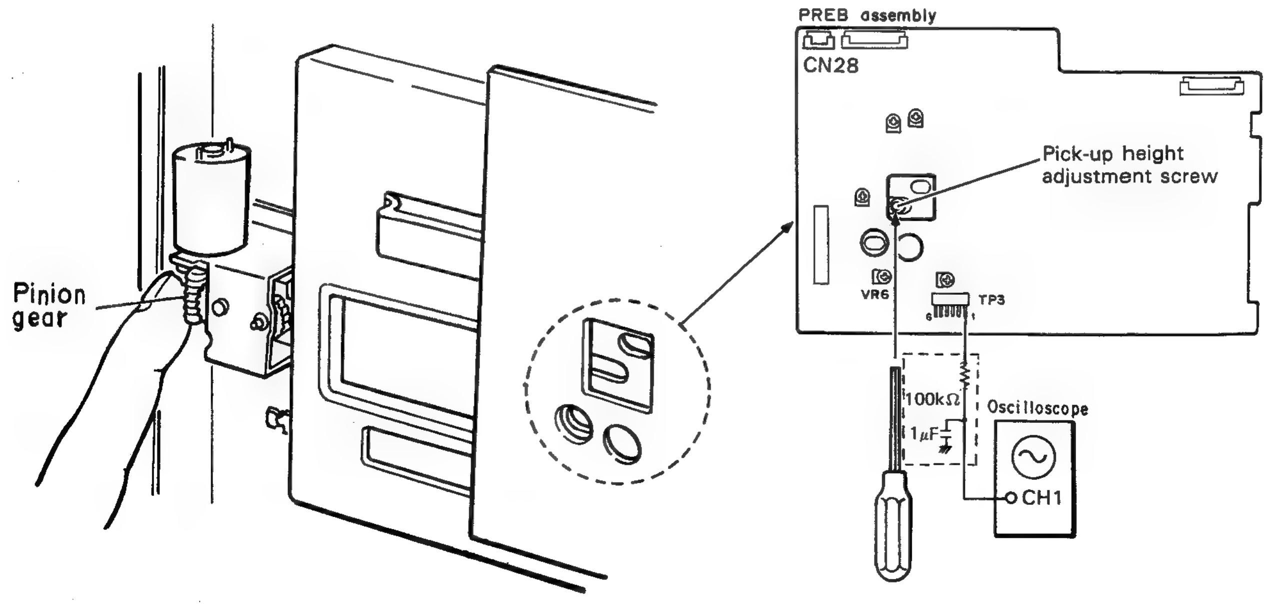


Fig. 3

4. PICK-UP TRACKING AND TANGENTIAL DIRECTION INCLINATION ADJUSTMENT

- Purpose: Adjust the inclination of the slider shaft so that the pick-up assembly moves parallel the disc, and then adjust the angle of the pick-up assembly in the tracking direction so that the laser beam strikes the disc perpendicularly (at a right angle).
- Symptoms when incorrectly adjusted: Crosstalk.

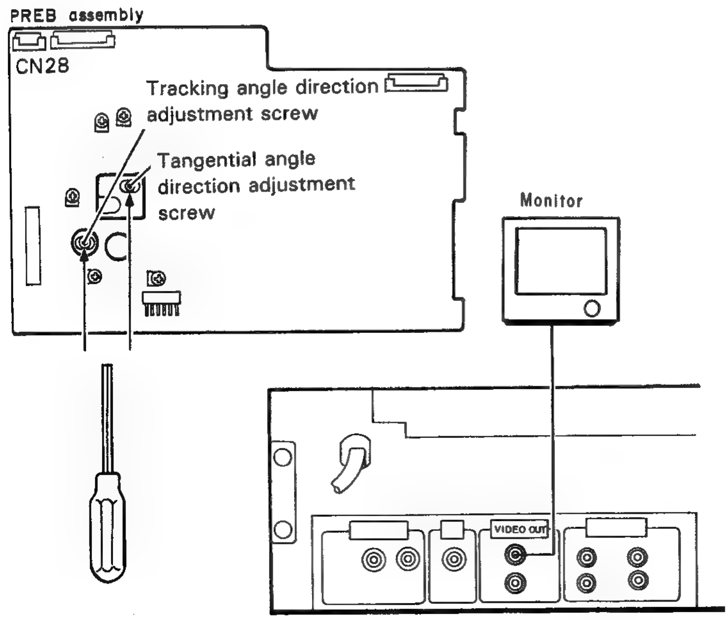
Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• TV monitor • Hexagonal wrench (2 mm) • Test disc: GGV1002	• TV monitor Connect to the video output terminal of the player.	* Normal mode: • Still mode • Tilt servo OFF (Unplug the connector of CN28)	• Tracking direction angle adjustment screw, tangential direction angle adjustment screw in the pick-up assembly.

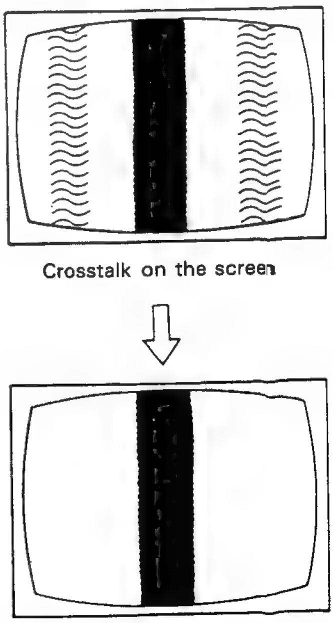
Adjusting procedure

Note: This adjustment should be performed with the unit placed horizontally.

1. Play the LD test disc and search for frame #115.
2. Rotate the tracking angle and tangential angle adjustment screws alternately and adjust repeatedly so that the crosstalk occurring on the right and left sides of the TV screen becomes minimum.

Adjustment diagram





Crosstalk on the screen

Minimum crosstalk

5. FOCUS ERROR BALANCE ADJUSTMENT

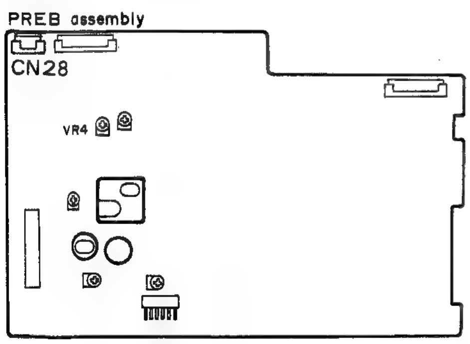
- Purpose: To set the object lens to its optimum position so that it works optimally with the focus servo while playing a disc.
- Symptoms when incorrectly adjusted: Crosstalk.

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• TV monitor • Test disc: GGV1002 • Oscilloscope	• TV monitor: Connect to the video output terminal of the player. • Oscilloscope: In the DADB assembly CH1: Between TRKG ERROR (TP2-2) and GND	* Service mode: • Play mode • Tracking servo loop open • Tilt servo OFF (Unplug the connector of CN28) * Normal mode: • Still mode • Tilt servo OFF	• VR4 in the PREB assembly

Adjusting procedure

1. Play the test disc in the service mode.
2. Around the position of frame #1,000, open the tracking servo, and adjust VR4 in the PREB asembly so that the tracking error signal waveform (TRKG ERROR) becomes maximum: write down the error level (A) at this time. (Fig. 5-1)
3. Set the player to the normal mode and search for frame #115.
4. Observe the crosstalk appearing on both the left and right sides of the TV screen, and check that the crosstalk is minimum and symmetrical. If crosstalk seems to be in good condition, this adjustment is finished.
5. If the crosstalk observed above is not acceptable, readjust VR4 in the PREB assembly to get minimum crosstalk. (Fig. 5-3)
6. Set the player to the service mode again, open the tracking servo around frame #1,000 and write down the error level (B) at this time. (Fig. 5-2)
7. When level difference between A and B is within 30% (B/A ≧ 0.7), this adjustment is finished.
8. If the level difference is more than 30%, return VR4 so that it becomes within 30%.
9. Set the player to the normal mode again and search for frame #115, and check that the crosstalk is minimum and symmertrial. (Fig. 5-3)
10. If the crosstalk seems in good condition, this adjustment is finished. If it is not acceptable, perform item "4. Pick-up tracking and tangential direction inclination adjustment" again. (See page 95)

Adjustment diagram



Tracking waveform

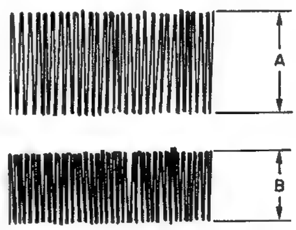
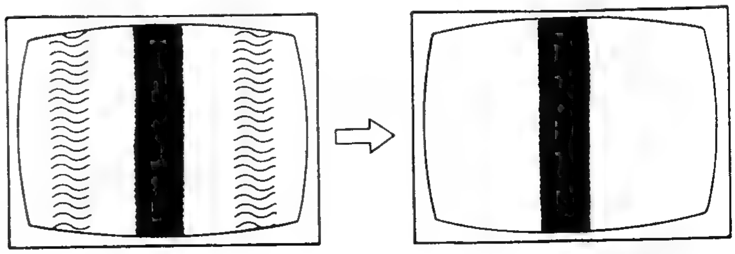


Fig. 5-1

Fig. 5-2



Crosstalk on the screen

Minimum crosstalk

Fig. 5-3

6. PICK-UP ASSEMBLY CENTERING CHECK

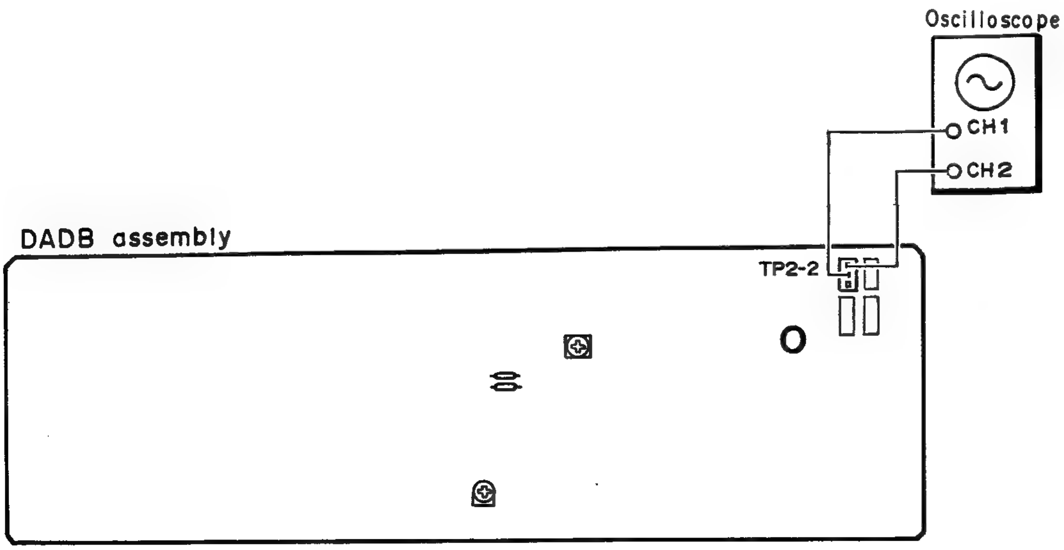
• Purpose: To check that the center of the spindle motor is on the track of the laser beam.

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Oscilloscope • Test disc: GGV1002	• Oscilloscope: In DADB assembly CH1 (X): Between TP2-2 (TRKG Error) and GND CH2 (Y): TP2-2 (TRKG A+C)	* Service mode: • Play mode • Tracking servo loop open • Tilt servo OFF (Unplug the connector of CN28)	

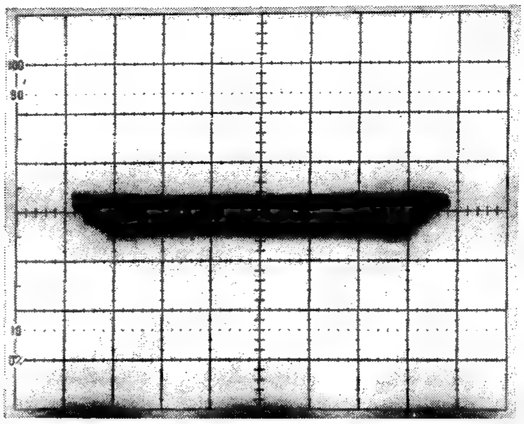
Adjusting procedure

1. With the player set horizontally, play the LD test disc.
2. After moving the pick-up toward inside of the disc using the Step keys, open the tracking servo.
3. Connect the X-input (CH1) of the oscilloscope to TP2-2 (TRKG ERROR) in DADB assembly and the Y-input (CH2) to TP2-2 (TRKG A+C).
   Set the oscilloscope to the X-Y mode, and observe the Lissajous waveform of the TRKG error signal and the TRKG A+C signal.
4. Record the Y-axis amplitude of the Lissajous waveform.
5. Close the tracking servo and move the pick-up toward the outside of the disc using the SCAN FWD keys. Then, open the tracking servo again, and observe the Lissajous waveform. At this time, check that the Y-axis amplitude of the Lissajous waveform is the same as the recorded one in step 4.
   If the Lissajous waveforms of the inside and outside of the disc are different in their Y-axis amplitude, perform "7. Pick-up Assembly Centering Adjustment". (See page 99)

Adjustment diagram



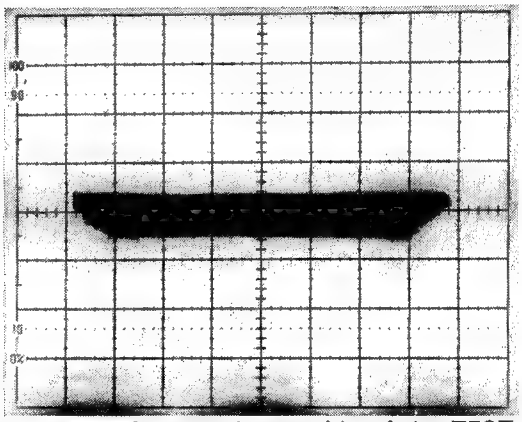
Waveforms
* Oscilloscope range:
CH1(X): 0.2V/div., DC input
CH2(Y): 0.2V/div., AC input
X-Y mode



Y Photo 3

Lissajous waveform at the inside of the TEST disc

Check that Y = Y'.



Y' Photo 4

Lissajous waveform at the outside of the TEST disc

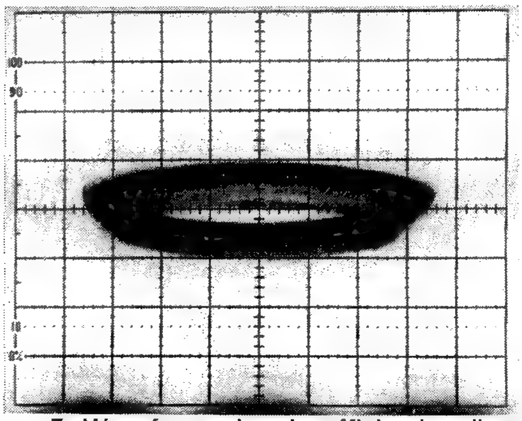


Photo 5: Waveform when insufficiently adjusted

7. PICK-UP ASSEMBLY CENTERING ADJUSTMENT

- Purpose: To adjust so center of the spindle motor comes on the track of the laser beam.
- Symptoms when incorrectly adjusted: Track jumping, longer search time.

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Oscilloscope • Short-shaft hexagonal wrench (2 mm) or, L-shaped hexagonal wrench • Test disc: GGV1002	• Oscilloscope: In DADB assembly CH1 (X): Between TP2-2 (TRKG Error) and GND CH2 (Y): TP2-2 (TRKG A+C)	* Service mode: • Play mode • Tracking servo loop open/close • Tilt servo OFF (Unplug the connector of CN28)	• Centering adjustment screw in the pick-up assembly

Adjusting procedure

Note: This adjustment should be performed only when the pick-up assembly is insufficiently adjusted by the "6. Pick-up assembly centering check". (See page 97)

1. Connect the X-input (CH1) of the oscilloscope to TP2-2 (TRKG ERROR) in DADB assembly and Y-input (CH2) to TP2-2 (TRKG A+C) respectively.
2. Play the test disc and search for frame #20,000 using the SCAN FWD key to move the pick-up towards the outside of the disc.
3. Open the tracking servo, and observe the Lissajous waveforms of the TRKG error signal and the TRKG A+C signal.
4. Fine adjust the grating so that the Y-axis amplitude of the Lissajous waveform becomes minimum. (Photo 7)
5. Close the TRKG servo and move the pick-up toward the inside of the disc by pressing the SCAN REV key.
6. Open the TRKG servo again, and observe the Lissajous waveform and record its Y-axis amplitude.
7. Move the pick-up toward outside again, and rotate the centering adjustment screw clockwise by 45° with the hexagonal wrench. (Fig. 4)
   Rotate the centering adjustment screw slowly so that the Y-axis amplitude of the Lissajous waveform decreases. After the Y-axis amplitude of the Lissajous waveform becomes minimum, rotate the hexagonal wrench further in the same direction until the Y-axis amplitude of the Lissajous waveform becomes the same level as the recorded one in step 6. (Photo 6 — 8)
8. Close the TRKG servo and move the pick-up toward the outside of the disc using the SCAN FWD key.
9. Repeat the operation in steps 3, 4 and 5.
10. Open the TRKG servo again to observe the Lissajous waveform, and check that the Y-axis amplitude is minimum.
    If the Lissajous waveform is expanded in the Y-axis direction, repeat the operation in steps 7, 8, 9, and 10.

Adjustment diagram

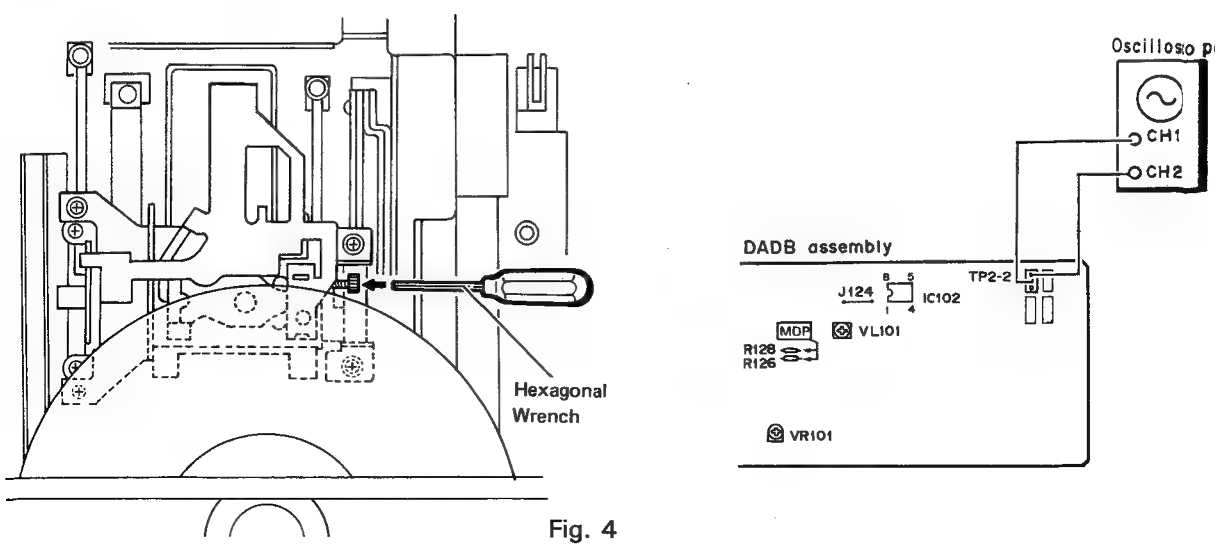


Fig. 4

Waveforms

*Oscilloscope range:
X: 0.2V/div., DC input
Y: 0.2V/div., AC input
X-Y mode

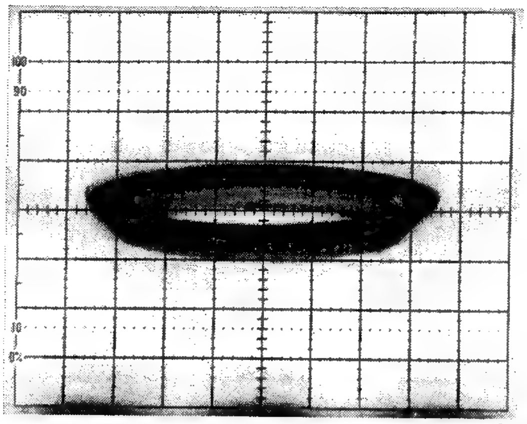


Photo 6

⇩

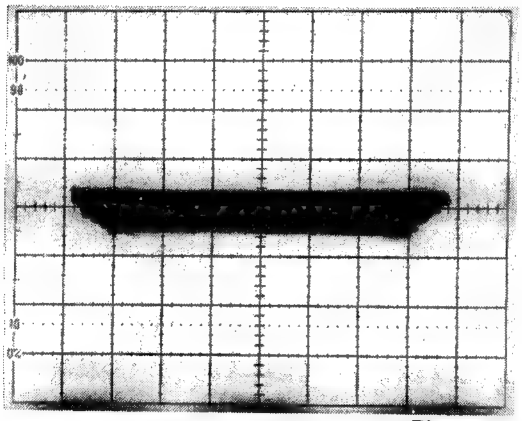


Photo 7

⇩

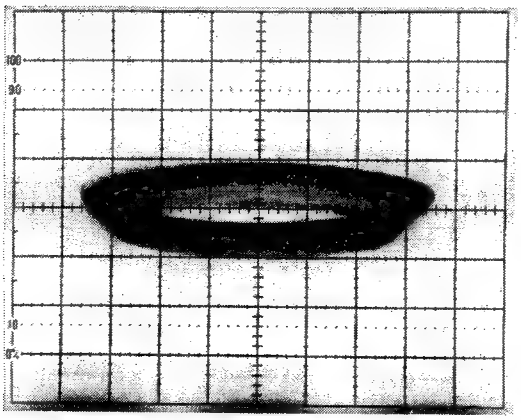


Photo 8

8. TILT STAY INCLINATION ADJUSTMENT

- Purpose: To set the electrical offset of the tilt servo to 0 V by adjusting the inclination of the tilt sensor.
- Symptoms when incorrectly adjusted: Crosstalk

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Oscilloscope • Test disc: GGV1002 • Philips ⊕ screwdriver	• Oscilloscope: In PREB assembly CH1: Between TP3-4 (TILT ERROR) and GND	# Normal mode: • Play mode • Tilt servo OFF (Unplug the connector of CN28)	• Tilt sensor inclination adjustment screw in the pick-up assembly

Adjusting procedure

Note: This adjustment should be performed with the unit placed horizontally.
This adjustment should be performed in the range of F# (frame numbers) 2000 – 10000 so the sensor output is not influenced by the mirror surface at the inside of the disc and external light at the edges of the disc.

1. Play the test disc and search for a position around frame #5000.
2. Connect the oscilloscope to TP3-4 in the PREB assembly, and observe the DC voltage of the tilt error signal.
3. Insert the small Philips ⊕ screwdriver with a long shaft from the rear panel of the player, and adjust the tilt sensor inclination adjustment screw so that the DC voltage of the tilt error signal becomes 0 V. (Fig. 5)
At this time, the above adjustment will be easy to perform when the pickup is locked by pressing the Multi Reverse key on the remote control.
4. Connect the connector CN28 which has been removed in "2. Grating Temporary Adjustment and Tracking Balance Adjustment". (See page 92)
5. Search for frame #115 and check that crosstalk at the left and right sides of the TV screen is minimum and symmetrical.

Adjustment diagram

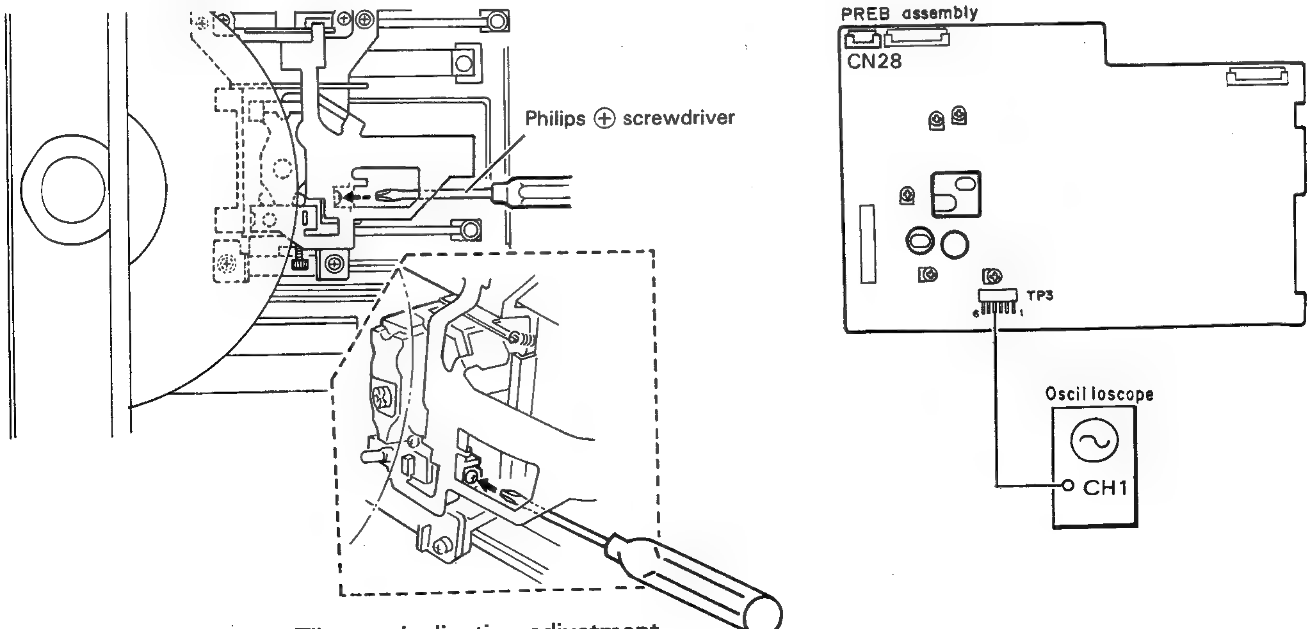


Fig. 5 Tilt stay inclination adjustment

9. GRATING FINE ADJUSTMENT AND TRKG BALANCE CHECK

- Purpose: To fine adjust the grating so that the two laser beams for TRKG (tracking) servo are emitted at the optimum track positions of the disc. Set the DC off-set voltage to 0V of TRKG Servo.
- Symptoms when incorrectly adjusted: Track jumping.

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Oscilloscope • Test disc: GGV1002 • Flat bladed ⊖ screwdriver	• Oscilloscope: In the DADB assembly CH1 (X): Between TP2-2 (TRKG ERROR) and GND CH2 (Y): TP2-2 (TRKG A+C)	* Service mode: • Play mode • Tracking servo loop open • Tilt servo OFF (Unplug the connector of CN28.)	• Grating adjustment screw in the pick-up assembly

Adjusting procedure

1. Play the LD test disc and search for frame #16,000, then open the TRKG servo.
2. Connect the X-input (CH1) of the oscilloscope to TP2-2 (TRKG ERROR) of the DADB assembly and Y-input (CH2) to TP2-2 (TRKG A + C) respectively. Set the oscilloscope to the X-Y mode, and observe the Lissajous waveform of the TRKG error signal and TRKG A + C signal.
3. Insert the flat-bladed small screwdriver into the grating adjustment hole, and fine adjust the grating so that the Y-axis dimension of the Lissajous waveform becomes minimum. (Fig. 6)
   At this time, if the grating is rotated excessively and the optimum point becomes unclear, perform "2. Grating Temporary Adjustment" again. (See page 92)
4. Select the X-input (CH1) of the oscilloscope, and check that the positive (A) and negative (B) amplitudes of the TRKG error signal are equal. (Photo 10)
   If the sizes of the positive and negative amplitude are different, perform "4. Pick-up Tracking and Tangential Direction Inclination Adjustment" again.
5. Close the TRKG servo loop and check that the picture on the TV screen is normal.

Adjustment diagram

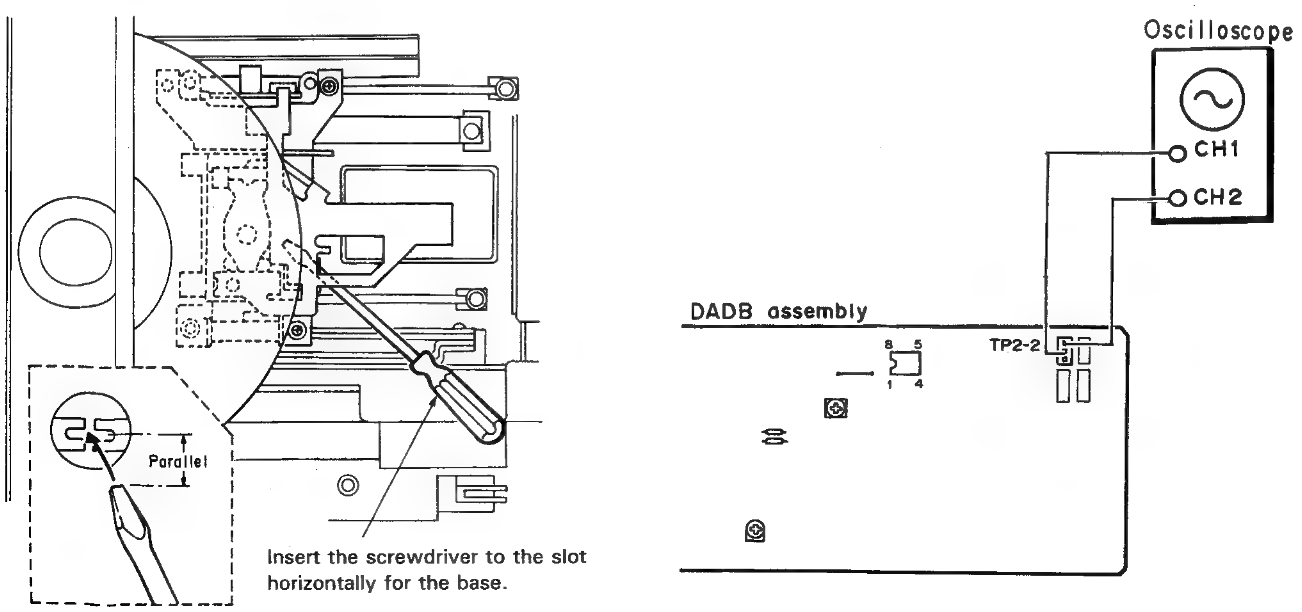


Fig. 6

Waveforms

- Oscilloscope range:
- ○ Grating adjustment
  CH1 (X): 0.2V/div., DC input
  CH2 (Y): 0.2V/div., AC input
  X-Y mode
- ○ TRKG balance adjustment
  CH1: 50 mV/div., 5 mS/div.

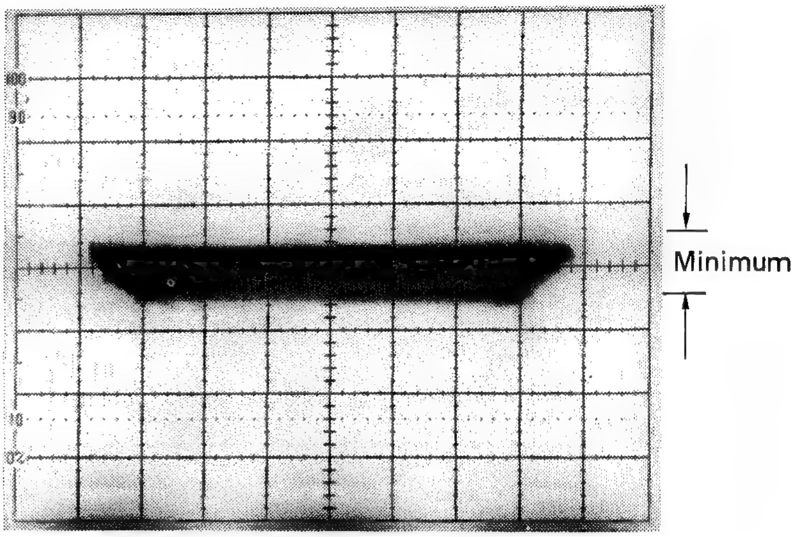


Photo 9 Grating Fine Adjustment

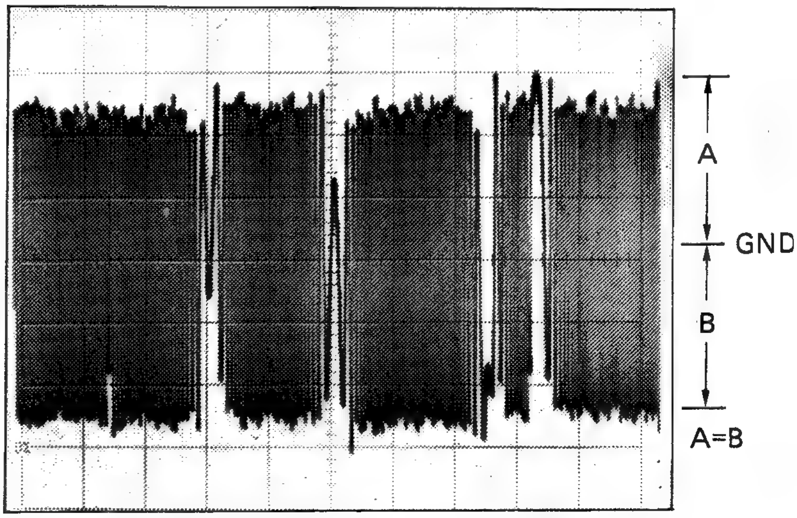


Photo 10 TRKG Balance Adjustment

10. RF GAIN ADJUSTMENT

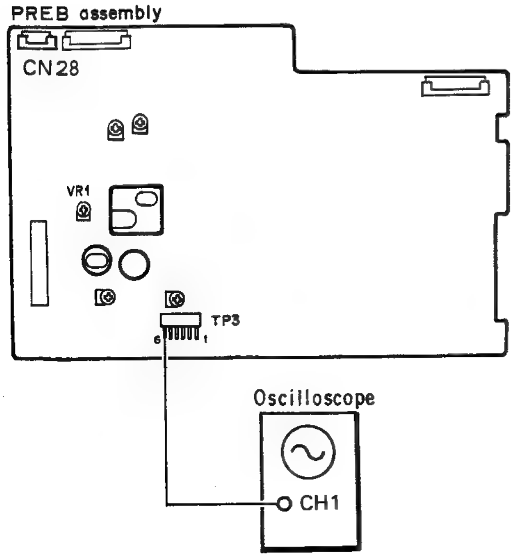
- Purpose: To set the amplitude of the RF signal to the optimum value.
- Symptoms when incorrectly adjusted: Dropout occurs frequently.

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Oscilloscope • Test disc: GGV1002	• Oscilloscope: In the PREB assembly CH1: Between TP3-6 (RF) and GND	* Normal mode: • Still mode • TILT servo OFF (Unplug the connector of CN28)	• VR1 in the PREB assembly

Adjusting procedure

1. Play the test disc and search for frame #15,000.
2. Connect the oscilloscope to TP3-6 in the PREB assembly to observe the RF signal.
3. Adjust VR1 in the PREB assembly so that the amplitude of the RF signal becomes 300 mV ±30 mV. (Photo 11)

Adjustment diagram



Waveforms

- Oscilloscope range: AC 10 mV/div., 5 mS/div.

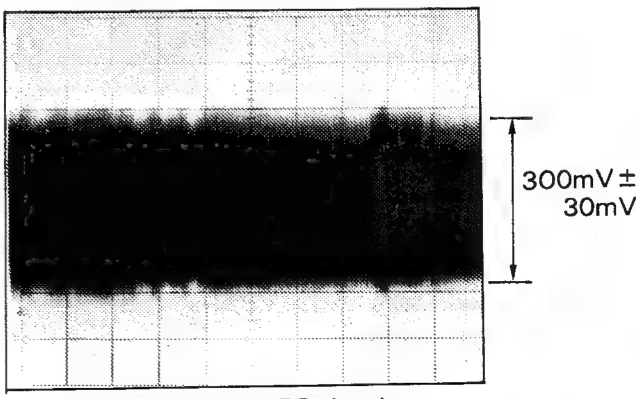


Photo 11 RF signal

11. H-SYNC SLICE ADJUSTMENT

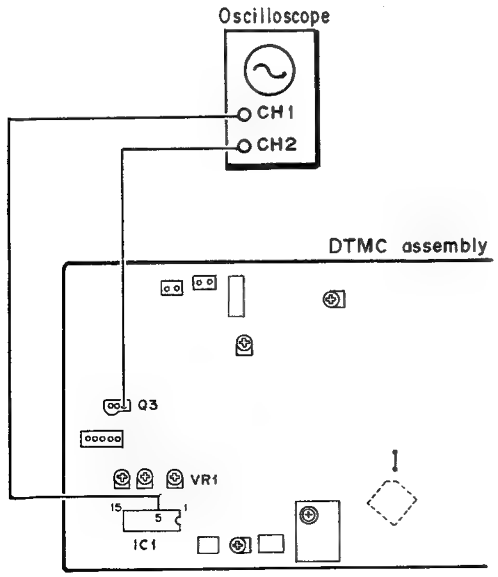
- Purpose: To add H-sync which can be shifted by up to 140 ns to the video memory signal output from memory.
- Symptoms when incorrectly adjusted: Spikes will appear when the H-sync of the video output signal rises.

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Oscilloscope • Test disc: GGV1002	• Oscilloscope: In the DTMC assembly CH1: Between IC1 pin 5 and GND CH2: Q3 emitter	* Normal mode: • Play mode	• VR1 in the DTMC assembly

Adjusting procedure

1. Play the test disc, and adjust VR1 so that the pulse width of the signal output from IC1 pin 5 becomes 4.3 μsec ± 0.1 μsec. At this time, check that the H-Sync of the Q3 emitter is sliced. Fine adjust VR1 so that the burst level of the input video signal is not lost. (Fig. 7)

Adjustment diagram



Waveforms

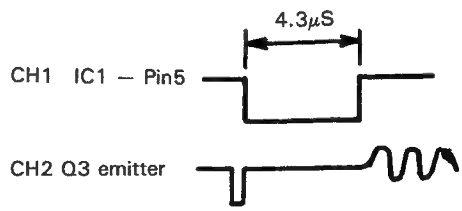


Fig. 7

12. BURST GATE TIMING ADJUSTMENT

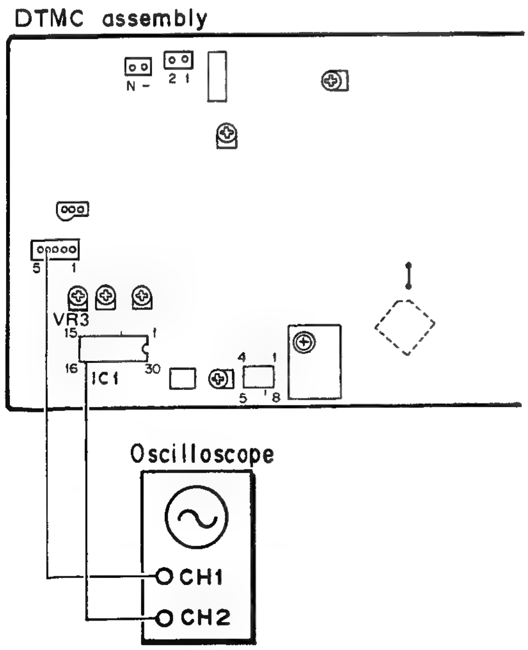
- Purpose: To set the burst gate to the optimum position.
- Symptoms when incorrectly adjusted: Play starts from the middle of the disc. No color, disordered color, significant stripes.

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Oscilloscope • Test disc: GGV1002	• Oscilloscope: In the DTMC assembly CH1: Between CN9 pin 4 and GND CH2: IC1 pin 16	* Normal mode: • Play mode	• VR3 in the DTMC assembly

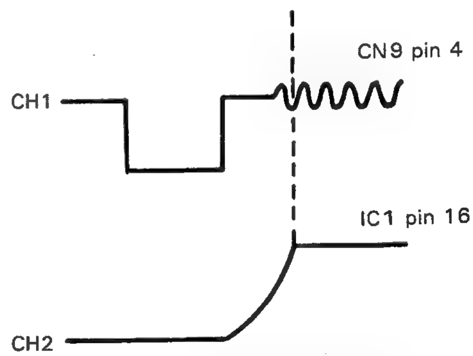
Adjusting procedure

1. Play the test disc.
2. Connect the CH1-input of the oscilloscope to CN9 pin 4 in the DTMC assembly and CH2-input to IC1 pin 16.
3. Adjust VR3 so that the rising edge of the pulse waveform of the output signal from IC1 pin 16 appears with the same timing as that of the first burst pulse of the video signal output from CN9 pin 4. (Fig. 8)

Adjustment diagram



Waveforms



The first burst of the video signal from CN9 pin 4 has the same timing as the rising edge of the pulse from IC201 pin 16.

Fig. 8

13. VCO OFFSET ADJUSTMENT

- Purpose: To set the VCO offset voltage (14.31818 MHz) to 0 V.
- Symptoms when incorrectly adjusted: Disordered picture and disordered horizontal scanning or no color during scanning of CLV disc.

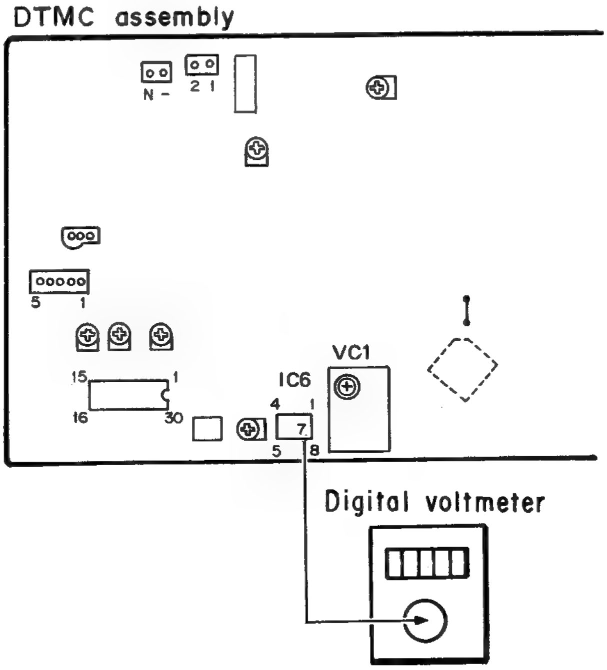
Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• DC voltmeter • Test disc: GGV1002	• DC voltmeter: In the DTMC assembly CH1: Between IC6 pin 7 and GND	* Normal mode: • Play mode (when PLL at the write side is locked)	• VC1 in the DTMC assembly

Adjusting procedure

1. Play the test disc.
2. Connect the DC voltmeter to IC6 pin 7, and adjust VC1 so that the DC level becomes 0 V ±100 mV.

Note: Disc playback becomes impossible, if the DC level is set far from the optimum voltage.

Adjustment diagram



14. TRAPEZOIDAL GAIN ADJUSTMENT

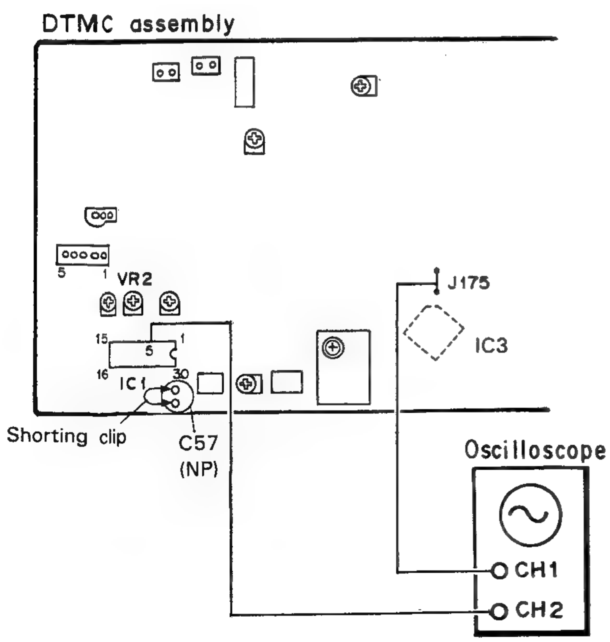
- Purpose: To adjust the inclination of the trapezoidal waveform for the spindle motor and TBC error detection.
- Symptoms when incorrectly adjusted: Flicker or displaced memory picture in through and still modes with CAV discs.

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Oscilloscope • Test disc: GGV1002 • Shorting clip	• Oscilloscope: In the DTMC assembly CH1: Between IC3 pin 1 (J175) and GND CH2: IC1 pin 5	* Normal mode: • Play mode (When the PLL on the Write side is locked)	• VR2 in the DTMC assembly

Adjusting procedure

1. With the PLL locked, short-circuit both ends of C57 in the DTMC assembly.
2. Connect the adjacent land of IC3 pin 1 (J175) to the CH1-input of the oscilloscope and IC1 pin 5 to CH2-input.
3. Adjust VR2 so that the falling edge of the signal at IC1 pin 5 comes at the center of the H period of the signal from IC3 pin 1. (Photo 12)

Adjustment diagram



Waveforms

* Oscilloscope range CH1, CH2: 2V/div, 10μS/div

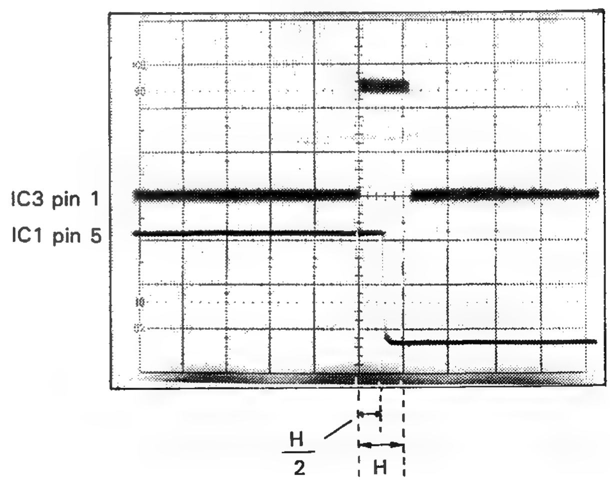


Photo 12

15. 140 nS SHIFT LEVEL ADJUSTMENT

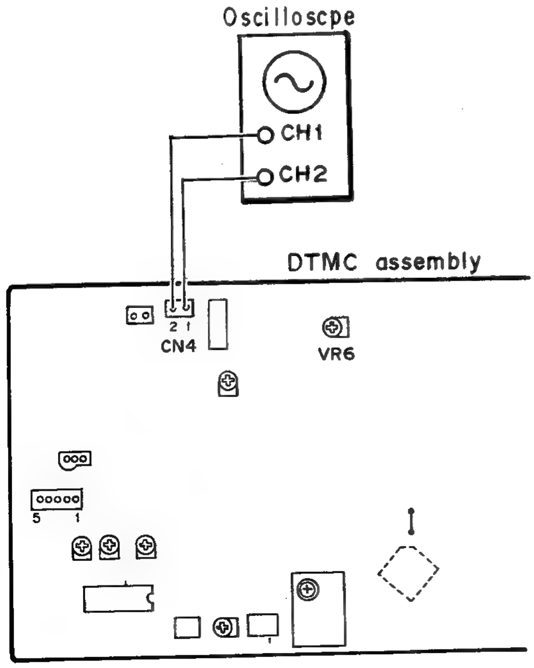
- Purpose: To set the chroma waveform amplitude of video signal which is shifted by 140 ns to the same level as the chroma waveform amplitude of the video signal which is not shifted.
- Symptoms when incorrectly adjusted: Flickering on the TV screen.

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Oscilloscope • Test disc: GGV1002	• Oscilloscope: In the DTMC assembly CH1: Between CN4 pin 2 and GND CH2: CN4 pin 1	* Normal mode: • Still mode	• VR6 in the DTMC assembly

Adjusting procedure

1. Connect CN4 pin 2 of the DTMC assembly to CH1 of the oscilloscope and CN4 pin 1 to CH2.
2. Play the test disc, and search for frame #7,201.
3. Trigger oscilloscope at the falling edge of output waveform at CN4 pin 2 (CH1).
4. Adjust VR6 in the DTMC assembly so that the period t1 shown in the waveform diagram (t1) becomes 140 nS±5nS.

Adjustment diagram



Waveforms

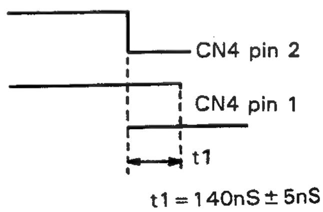


Fig. 9

16. SYNC LEVEL ADJUSTMENT

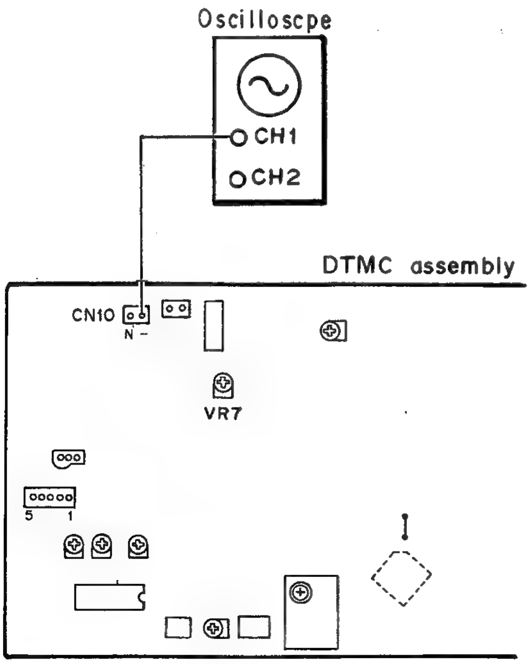
- Purpose: To adjust to the standard video signal (140 IRE)
- Symptoms when incorrectly adjusted: Picture will be distorted.

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Oscilloscope or waveform monitor • Test disc: GGV1002	• Oscilloscope: In the DTMC assembly CH1: Between CN10 pin 1 and GND	* Normal mode: • Play mode	• VR7 in the DTMC assembly

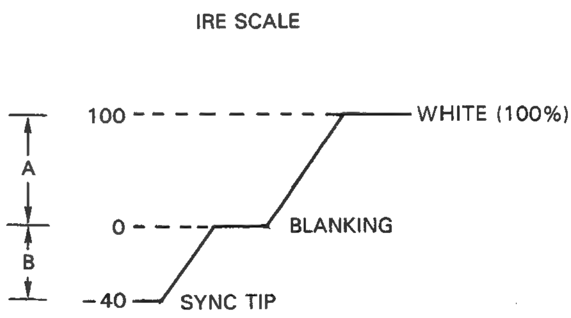
Adjusting procedure

1. Connect the oscilloscope to CN10 pin 1 in the DTMC assembly.
2. Observe the waveform at CN10 pin 1, and adjust VR7 so that the H (horizontal) sync level of the video signal becomes 40 IRE.

Adjustment diagram



Waveforms



$$\frac{B}{A+B} = \frac{40}{140}$$

17. MEMORY INPUT VIDEO LEVEL ADJUSTMENT

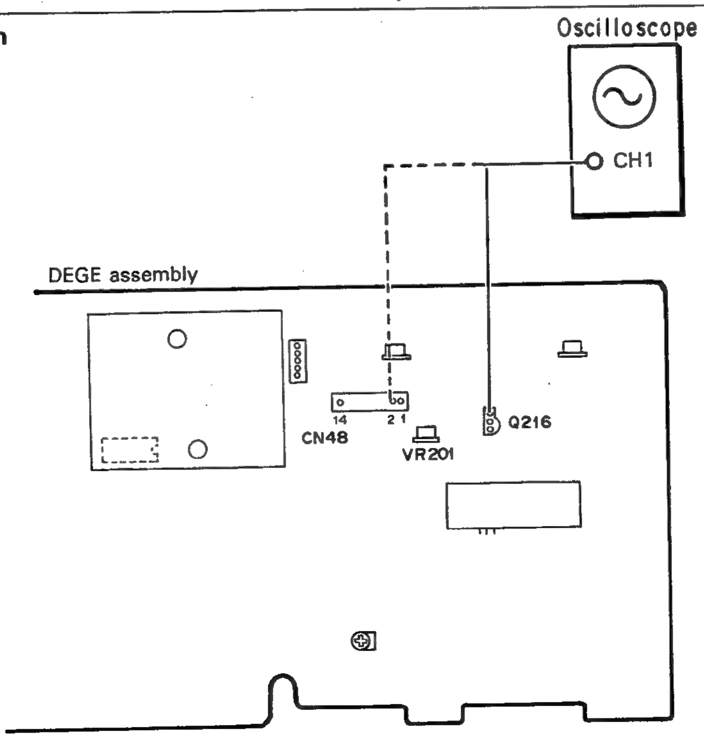
- Purpose: Adjustment of the video level for the A/D converter
- Symptoms when incorrectly adjusted: At "20. OUTPUT VIDEO LEVEL ADJUSTMENT", it cannot be adjusted to 1 Vp-p (with 75-ohm terminal resistor)

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Oscilloscope • Test disc: GGV1002	• Oscilloscope: In the DEGE assembly CH1: Between Q216 emitter (or CN48 pin 2) and GND	* Normal mode: • Play mode	• VR201 in the DEGE assembly

Adjusting procedure

1. Connect the oscilloscope to the emitter of Q216 (or CN48 pin 2) to observe the waveform.
2. Adjust VR201 in the DEGE assembly so that the peak-to-peak value from the white peak level to the sync tip level of the video signal waveform becomes 1.6 Vp-p.

Adjustment diagram



18. 1H DELAY VIDEO LEVEL ADJUSTMENT

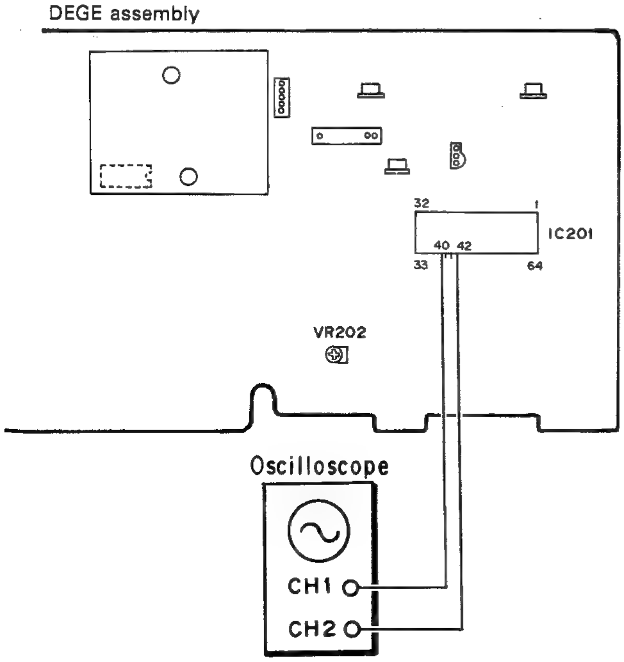
- Purpose: To set the amplitude of the 1H delayed video signal to the same level as the amplitude of the main video signal.
- Symptoms when incorrectly adjusted: When 1H delay level is high: White dropout is significant, and horizontal shift.
  When 1H delay level is low: Black dropout is significant.

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Oscilloscope • Test disc: GGV1002	• Oscilloscope: In the DEGE assembly CH1: Between IC201 pin 40 and GND CH2: IC201 pin 42	* Normal mode: • Play mode	• VR202 in the DEGE assembly

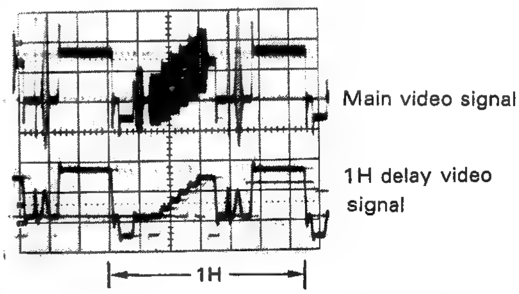
Adjusting procedure

1. Play the test disc and search for frame #19,801.
2. Connect CH1 of the oscilloscope to IC201 pin 40 in the DEGE assembly and CH2 to IC201 pin 42, and observe the waveform of the main video signal and the 1H delayed video signal at the same time.
3. Adjust VR202 in the DEGE assembly so that the amplitude from the sync tip level to the white peak level of the 1H delay video signal (CH2) becomes the same as that of the main video signal. (Photo 13)

Adjustment diagram



Waveforms



CH1: 50 mV/div., DC input
CH2: 50 mV/div., DC input
10 μS/div.

Photo 13

19. VPS ERROR SIGNAL INJECTION LEVEL ADJUSTMENT

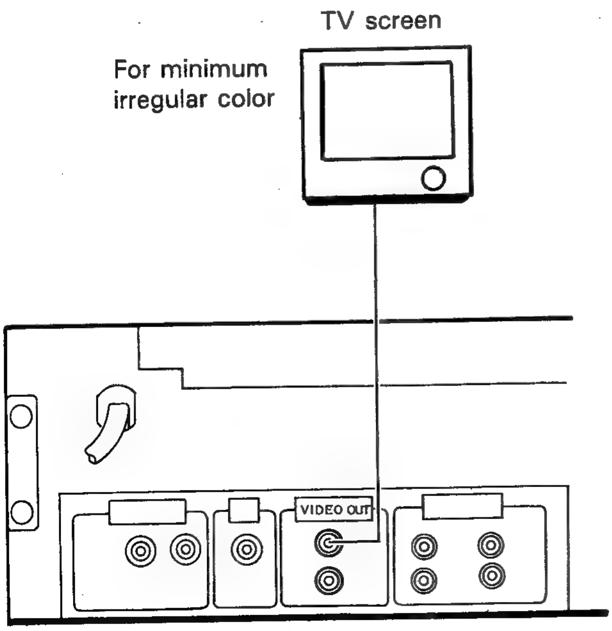
- Purpose: To set the amount of injection of the color phase error signal to the color phase error compensation section to the optimum value.
- Symptoms when incorrectly adjusted: Irregular color becomes significant.

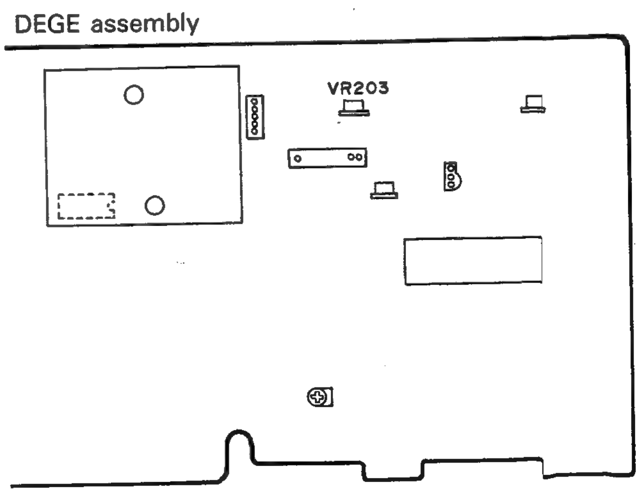
Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• TV monitor • Test disc: GGV1002	• TV monitor Connect to the video output terminal of the player.	* Normal mode: • Still mode	• VR203 in the DEGE assembly

Adjusting procedure

1. Play the test disc and search for frame #7,201.
2. Adjust VR203 in the DEGE assembly so that irregularities on the magenta screen become minimum.

Adjustment diagram





20. OUTPUT VIDEO LEVEL ADJUSTMENT

- Purpose: To set the output video signal level to 0.714 Vp-p.
- Symptoms when incorrectly adjusted: Video data readout incomplete, and play starts from the middle of the disc. TV screen is too bright or too dark.

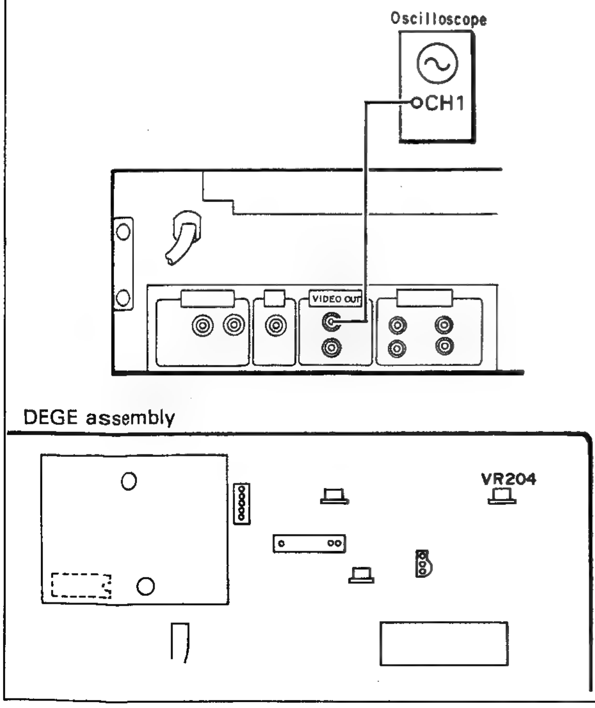
Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Oscilloscope • Test disc: GGV1002	• Oscilloscope: Connect to the video output terminal of the player.	* Normal mode: • Play mode	• VR204 in the DEGE assembly

Adjusting procedure

Note: The video output terminal is regarded as being terminated with 75 ohms when it is connected to a TV monitor.

1. Play the test disc and search for frame #19,801.
2. Connect the oscilloscope to the video output terminal on the DEGE assembly to observe the playback video signal waveform.
3. Adjust VR204 so that the amplitude from the pedestal level to the white level of the playback video signal waveform becomes 0.714 Vp-p. (Photo 14)

Adjustment diagram



Waveforms

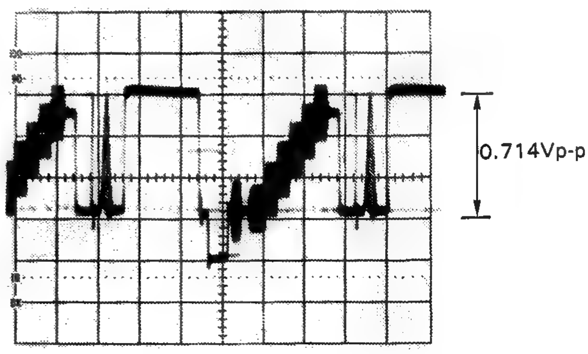


Photo 14

21. 4FSC VCXO ADJUSTMENT

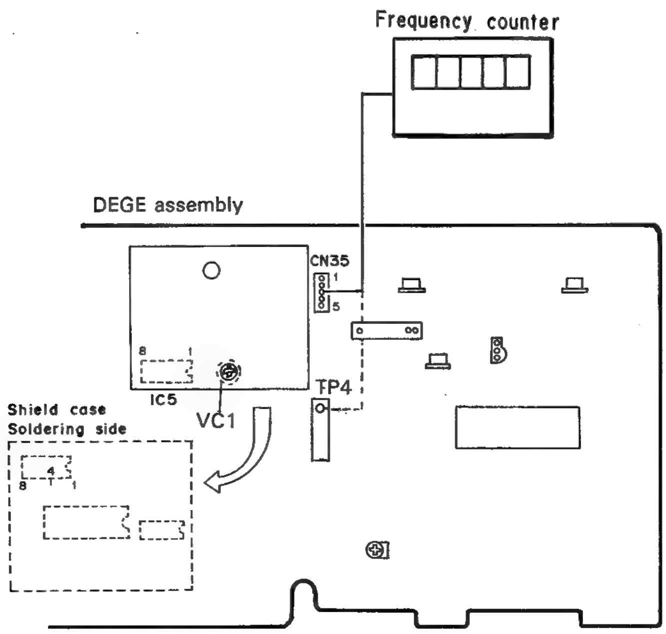
- Purpose: To adjust the reference clock frequency of the 4fsc system to the correct value.
- Symptoms when incorrectly adjusted: Sync not possible. Initialization impossible.

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Frequency counter	• Frequency counter: Between CN35 pin 3 (or TP4) and GND.	* Normal mode: • Stand-by mode	• VC1 in the DEGE assembly

Adjusting procedure

1. Connect the frequency counter to CN35 pin 3 (or TP4) of the DEGE assembly.
2. Adjust VC1 of the DEGE assembly so that the frequency counter readout becomes 14.31818 MHz ±50 Hz.

Adjustment diagram



22. 260 fH VCO ADJUSTMENT

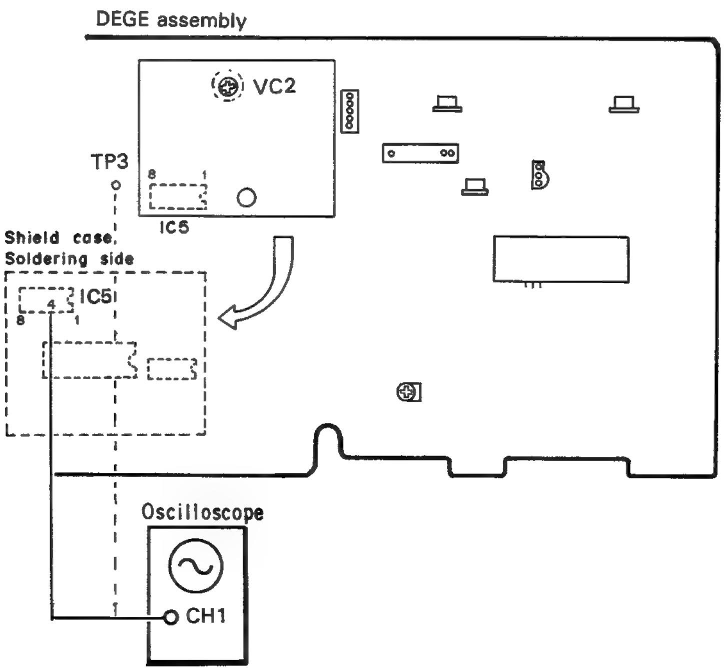
- Purpose: Adjustment of optimum operating point of PLL.
- Symptoms when incorrectly adjusted: Sync not possible. Initialization impossible.

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Oscilloscope • Test disc: GGV1002	• Oscilloscope: In the DEGE assembly CH1: Between IC5 pin 4 (or TP-3) and GND	* Normal mode: • Stand-by mode	• VC2 in the DEGE assembly

Adjusting procedure

1. Connect the oscilloscope to IC5 pin 4 (or TP3) in the DEGE assembly to observe the waveform.
2. Play the test disc, and adjust VC2 in the DEGE assembly so that the voltage becomes 3.2 V ±0.16 V.

Adjustment diagram



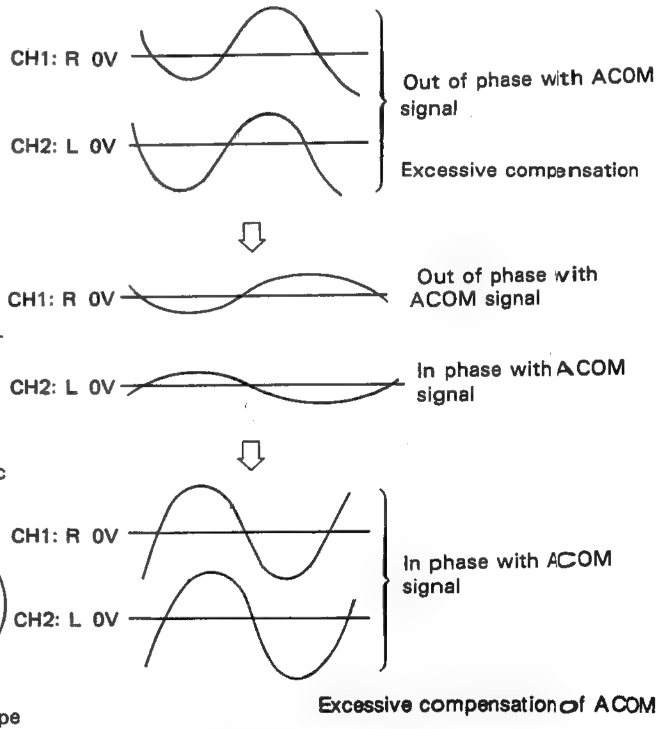
23. ACOM INSERTION LEVEL ADJUSTMENT

Purpose: To correct the timebase of audio playback signal.
Symptoms when incorrectly adjusted: Degraded S/N of audio signal when CX is OFF.

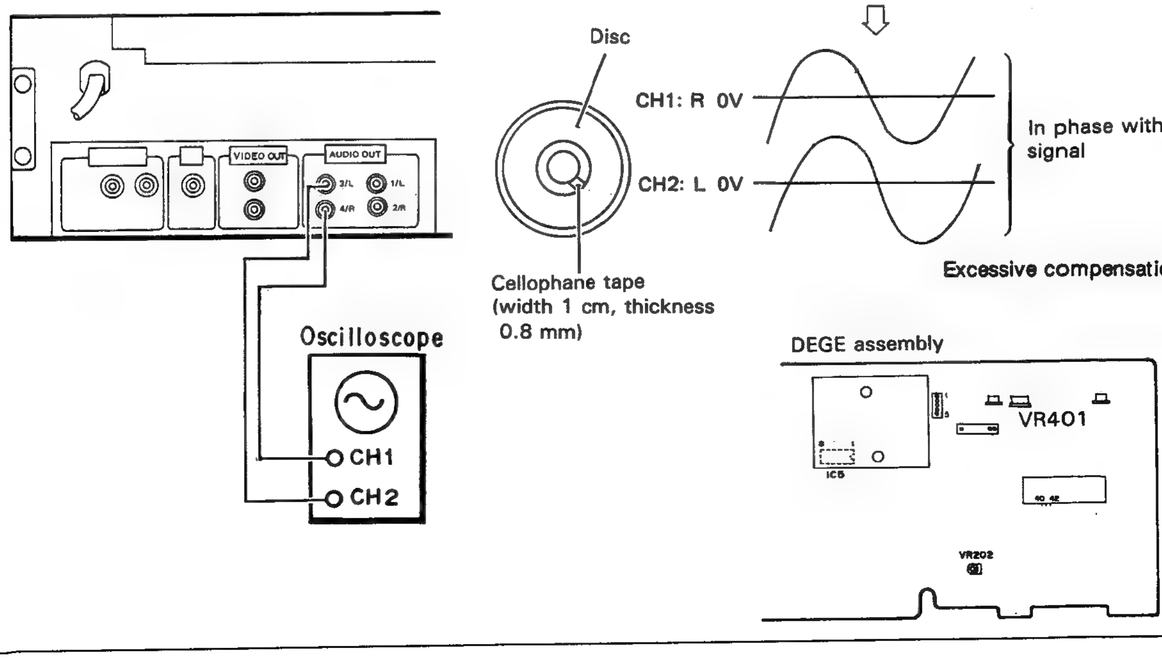
Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Test disc: GGV1002 (Attach cellophane tape approx. 1 cm width and 0.8 mm thickness to the center hole of the disc.) • Oscilloscope	• Oscilloscope: Main unit AUDIO OUT (ANALOG 3/L, 4/R) terminals	* Normal mode: • PLAY mode	• VR401 in the DEGE assembly

Adjusting procedure

1. Attach cellophane tape with a width of approx. 1 cm and thickness of 0.8 mm to the center hole of the test disc to make the disc eccentric.
2. Connect the oscilloscope to the AUDIO OUT (ANALOG 3/L, 4/R) terminals of the main unit.
3. Play back around frame #18,901 of the test disc and observe the waveform on the oscilloscope.
4. At this time, the left and right channel waveforms should be adjusted to be equal and minimum.



Adjustment diagram



24. DECODER CLOCK ADJUSTMENT

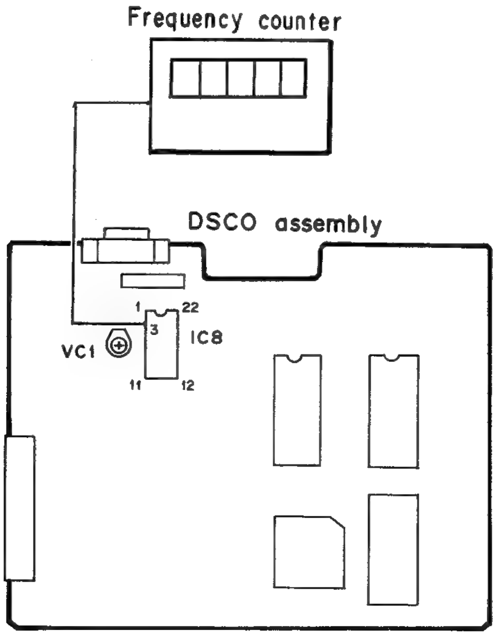
- Purpose: To set the decoder clock frequency to its optimum value.
- Symptoms when incorrectly adjusted: Longer search time.

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Frequency counter	• Frequency counter: In the DSCO assembly Between IC8 pin3 and GND	* Service mode: (When nothing is input, the message OSC ON will be displayed on the screen.)	• VC1 in the DSCO assembly

Adjusting procedure

1. Set the Service Mode and connect the frequency counter to IC8 pin 3 in the DSCO assembly.
2. When OSC ON is displayed on the screen, adjust VC1 in the DSCO so that the frequency becomes 3.0 MHz ±50kHz.

Adjustment diagram



25. PLL FREE-RUNNING ADJUSTMENT

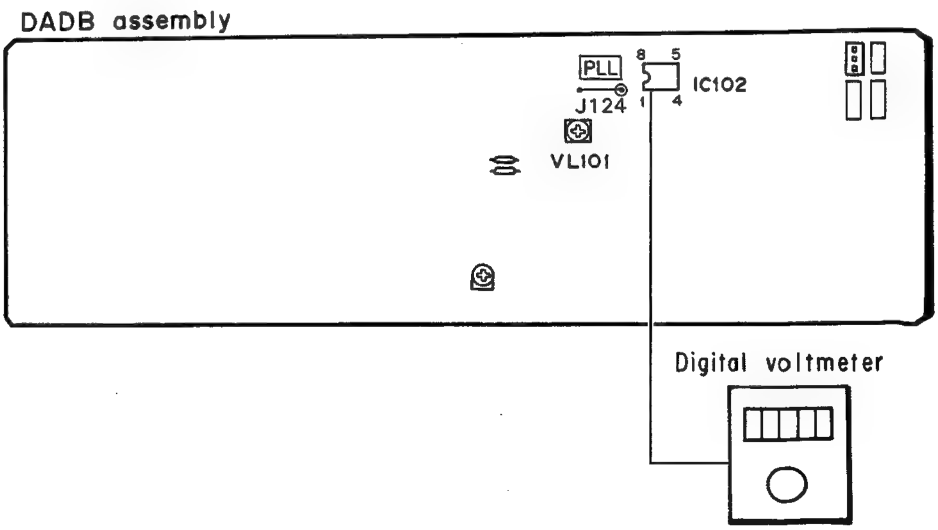
- Purpose: To adjust the VCO free-running frequency for the PLL in the EFM decoder to the optimum value.
- Symptoms when incorrectly adjusted: No sound, or sound interrupted.

Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Digital voltmeter • 8-inch LDD (LD disc with digital audio) disc (commercial available)	• Digital voltmeter: In the DADB assembly Between IC102 pin 1 (or J124) and GND.	* Normal mode: • Play mode	• VL101 in the DADB assembly

Adjusting procedure

1. Play the 8-inch LDD disc.
2. Connect the digital voltmeter to IC102 pin 1 (J124) in the DADB assembly, and observe the DC voltage of the VCO control signal.
3. Adjust VL101 in the DADB assembly so that the DC voltage of the VCO control signal becomes 400 mV ±100 mV.

Adjustment diagram



26. VCXO OFFSET ADJUSTMENT

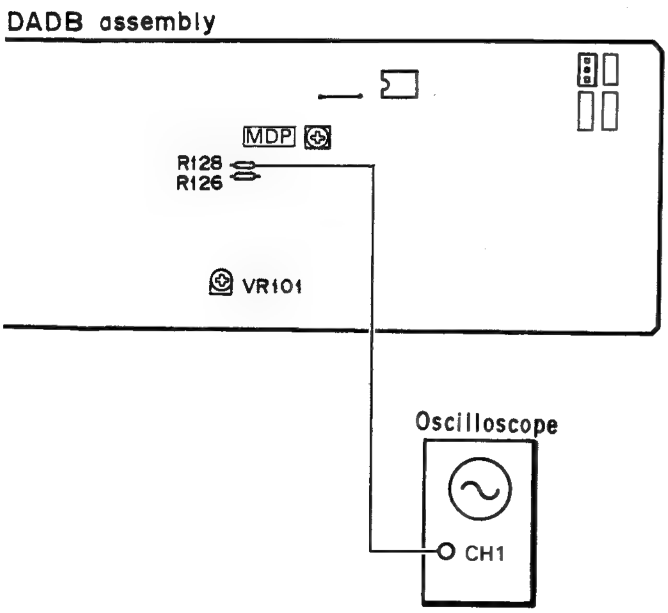
- Purpose: To set the offset voltage of the VCXO PLL phase error signal to minimum.
- Symptoms when incorrectly adjusted: Digital audio output interrupted when playing LDD disc (synchronous noise).

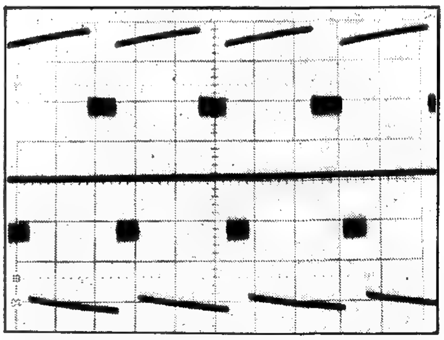
Measurement equipment & jigs	Measurement equipment connecting points	Player condition	Adjusting points
• Oscilloscope • 8-inch LDD (LD disc with digital audio) disc (commercially available)	• Oscilloscope: In the DADB assembly CH1: Between R128 lead wire (MDP) and GND.	* Normal mode: • Play mode	• VR101 in the DADB assembly

Adjusting procedure

1. Play the 8-inch LDD disc.
2. Connect the oscilloscope to the lead wire of R128 and observe the PLL phase error output signal of the VCXO.
3. Adjust VR101 in the DADB assembly so that the pulse-width at the positive or negative side becomes minimum and the waveform appears continuously.

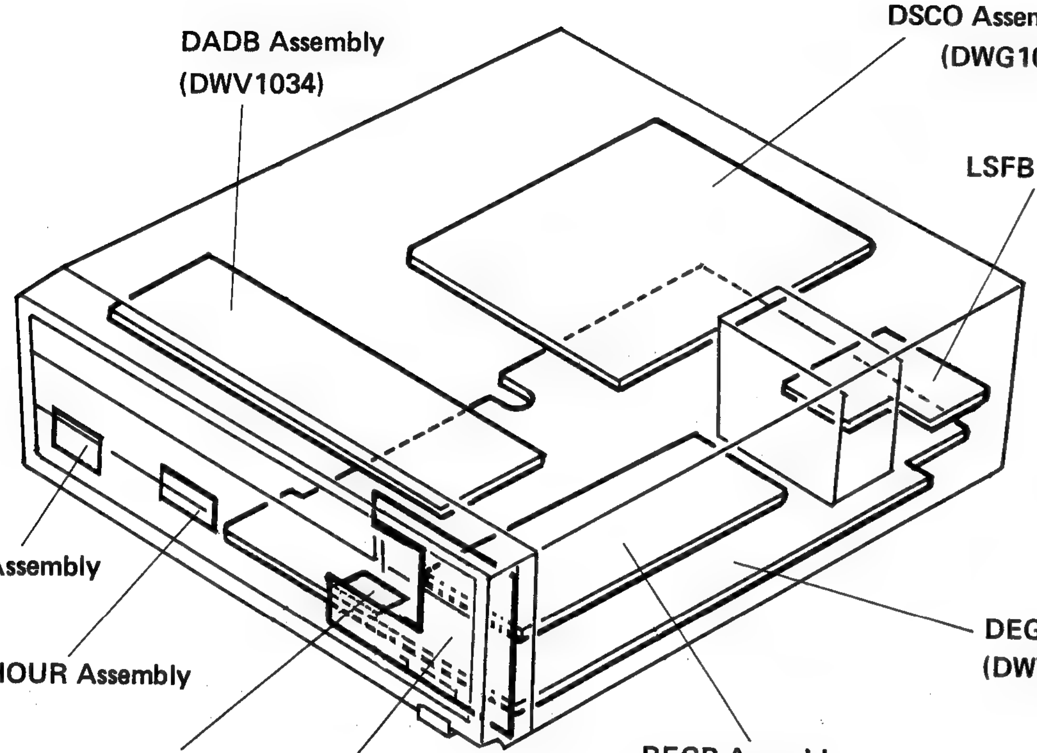
Adjustment diagram

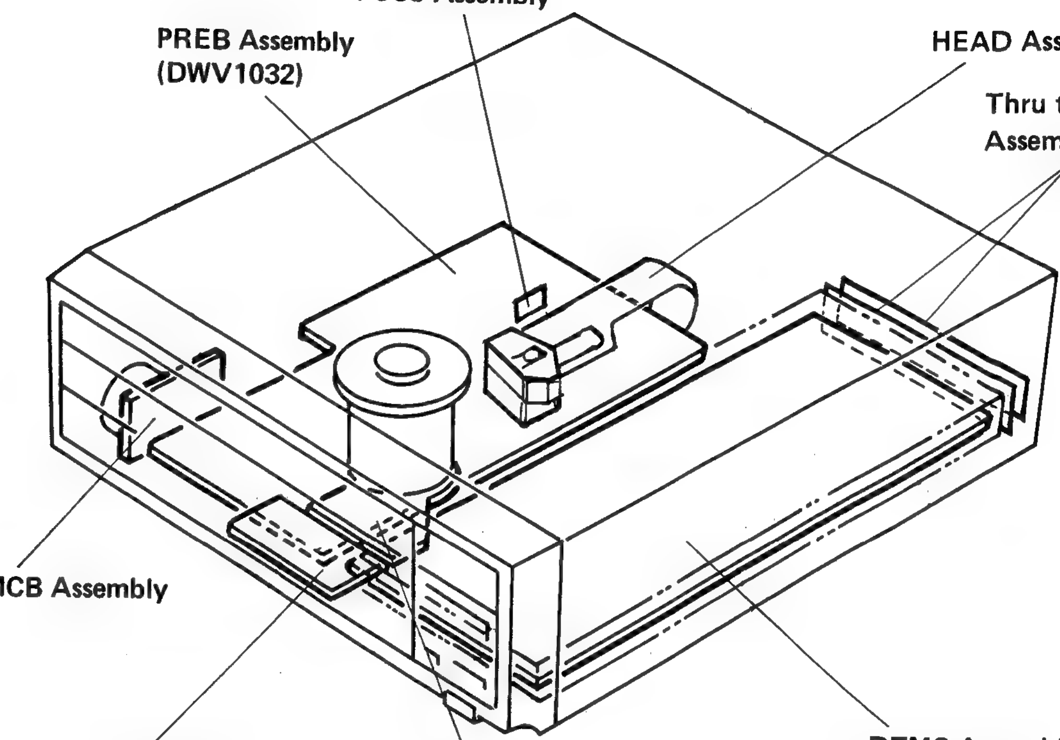




So that pulse-width is minimum and the waveform appears continuously.

10. P.C. BOARDS LOCATIONS





DSCO	Digital Signal Prosessor & Control
JACK	Jack Board
KEYB	Key Board
HOUR	Hour Meter
PWID	Power Indicator
REGB	Regurator Board
LSFB	Line Surge Filter Board
DEGE	Demodulation & Sync generation
DADB	Digital Audio Demodurator Board
DTMC	Digital Time base correcter & Memory Control

BLDB	Brushless Motor Drive Board
PREB	Pre Board
POSS	Position Sensor
HEAD	Head Board
LMCB	Loading Motor Control Board
BLMB	Brushless Motor Board

11. PANEL FACILITIES

PARK indicator

Indicates that the pickup is at the park position (extreme inner circumference) and in standby status.
Blinks during opening/closing operation of the disc table, and goes off when opening/closing is completed. It lights up when a disc exists in the player.

PLAY indicator

Lights during playback.

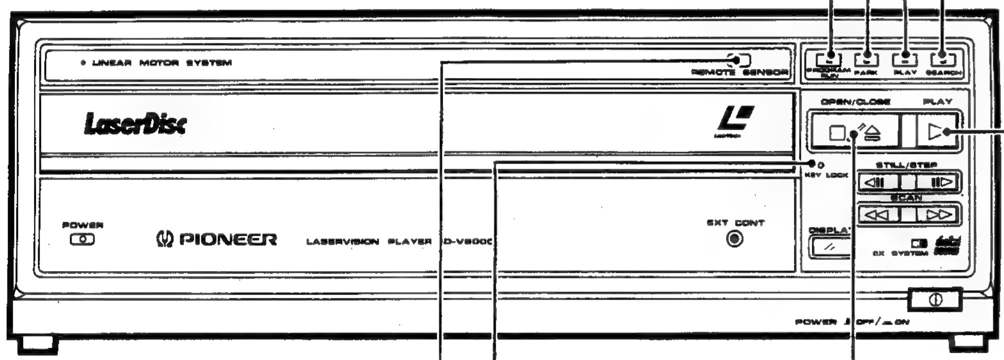
SEARCH indicator

Lights during execution of search.

PROGRAM RUN indicator

Lights during program playback.
Except in playback mode, the indicator lights up when dump mode is set (AUDIO 2/R ON).

PLAY (►) button



REMOTE SENSOR window

When using the optional remote control unit in the wireless format, the infrared commands from the unit are received here.

OPEN/CLOSE (■ / ≜) button

This button is used to open and close the disc table. Setting a disc on the disc table then pressing this button retracts the disc table into the player. Pressing this button during play stops play. When pressed again, the table will be extended from the player.

KEY LOCK indicator

Lit when the KEY LOCK command is entered from the external control unit.
When this indicator is lit, entries are not accepted from operation keys other than the power switch. Also, entries are not accepted from the operation keys of the separately sold remote control unit.

SCAN (◄◄, ►►) button

This is for quickly finding a particular point in the program from which you wish to play the disc. Scanning continues for as long as you keep the SCAN button depressed.
►►: Forward direction
◄◄: Reverse direction

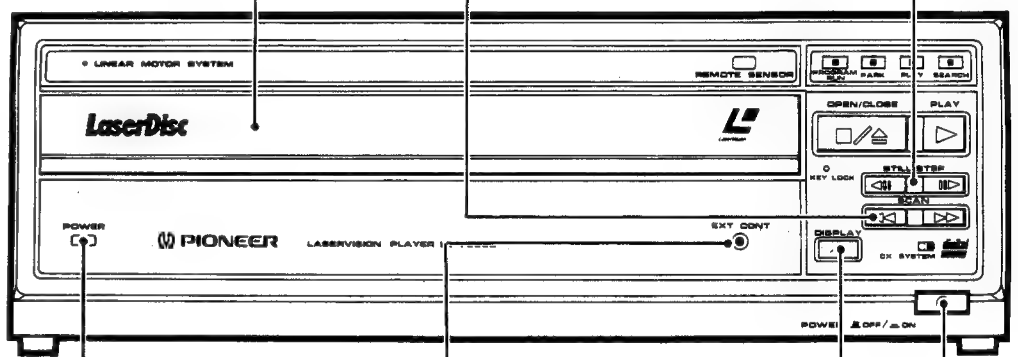
STILL/STEP (◄II, II►) button

When either end of the button is pressed, the unit will enter frame-by-frame playback. Then, when the II► end is pressed, the picture will advance forward frame-by-frame. When the ◄II end is pressed, the picture will reverse frame-by-frame.

NOTE:
On some CLV discs on which a second code is not recorded, the picture cannot be advanced forward or reverse frame-by-frame.

DISC TABLE

When power is switched on, and OPEN/CLOSE button is pressed, the disc table is expelled outward.



POWER indicator

When power is turned on, the indicator lights up.

POWER switch

Press this button to turn the power on and off.

EXT CONT terminal (stereo miniature phone jack)

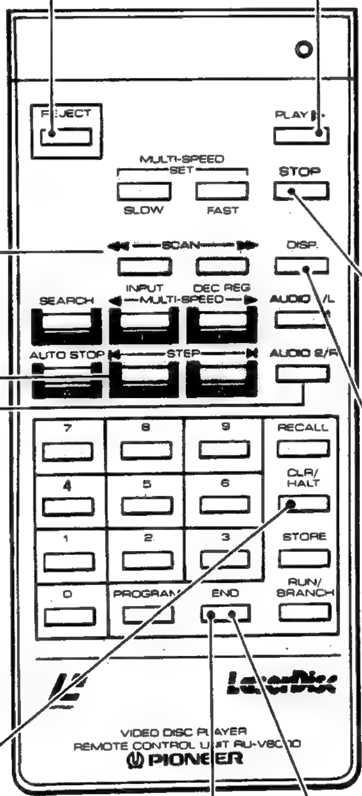
A terminal for connecting a separately sold remote control unit RU-V6000.

DISPLAY button

This button is used to display or erase chapter number and frame numbers on the TV screen.
When the power is turned ON with this button pressed, the function switches to setting mode.

NOTES
- *During CLV disc playback, elapsed time numbers will be displayed in place of frame numbers.*
- *When only the DISPLAY button is pressed, the display appears and reappears alternately each time the button is pressed.*

OPERATION WITH THE OPTIONAL REMOTE CONTROL UNIT



REJECT

When this button is pressed, playback ceases and the player enters the reject mode. The pickup returns to the standby position and disc rotation stops, but the disc table is not open.

SCAN

These are for quickly finding a particular point in the program from which you wish to play the disc. Scanning continues for as long as you keep the SCAN button depressed.
►►: Forward direction
◄◄: Reverse direction

STEP

Pressing either of the STEP buttons will produce a still video image. Then each time you press the ► marked STEP button, the image will advance to the next frame, each time you press the ◄ marked STEP button, the image will go backwards to the preceding frame.

AUDIO 1/L, 2/R

These are ON/OFF buttons for the two audio channels.

- Output during playback when audio is in the ordinary play mode or with AUTO STOP operating. Not output during trick play such as freeze frame, multi-speed, etc.
- When playing back the audio from one channel with a stereo device, the sound will be output from both speakers.
- When only the AUDIO 1/L, 2/R button is pressed, the sound from that channel is turned on and off alternately each time the button is pressed.

CLR

When you have inadvertently pressed the wrong digit button, press the clear (CLR) button to release the setting.

TIME/FRAME/CHAP.

- **When using extended play discs**

For setting search and auto stop operations in time, frame or chapter modes.
Whenever this button is pressed, the mode will be changed to time, frame and chapter modes in sequence.
When the power is turned on, this function is always set to time mode.

PLAY (►)

To begin playing a disc or resume play after another playback mode, press this button.

STOP

The image is frozen when this button is pressed.

DISP

This button is used to display or erase chapter number and frame numbers on the TV screen.

NOTES

- *During CLV disc playback, elapsed time numbers will be displayed in place of frame numbers.*
- *When only the DISP button is pressed, the display appears and reappears alternately each time the button is pressed.*
  The display can be made to appear and disappear directly by pressing a DIGIT button and the [DISP] button.
  Even number + [DISP]: delete
  Odd number + [DISP]: display

FRAME/CHAP.

- **When using standard play disc**

For setting search and auto stop operations in frame or chapter modes.
Pressing this button while the frame and chapter number are displayed will switch between the frame and chapter modes.
When the power is turned on, this function is always set to frame mode.

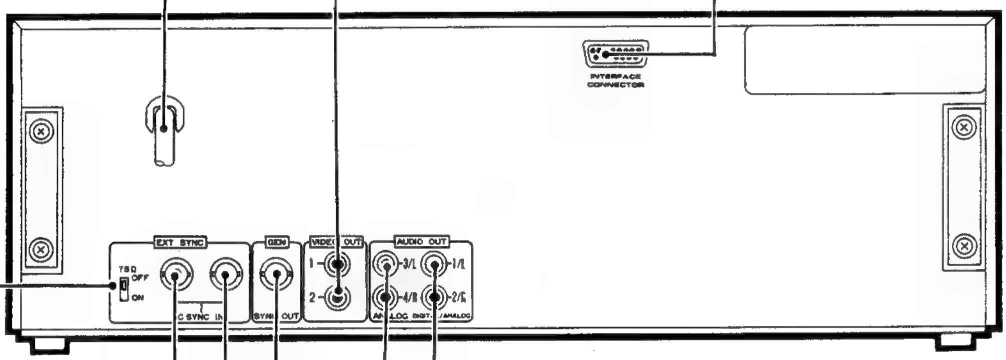
REAR PANEL FACILITIES

EXT SYNC TERMINATION selector
This switch is used for selecting whether the signal input to EXT SYNC is given 75Ω termination within the player (ON position), or looped through (OFF position).

Power cord
Plug this into wall outlet (120V, 50/60 Hz).

VIDEO OUTPUT terminals
These terminals are only for connection to a color video TV monitor (one which has a video input terminal). It provides an NTSC video signal. These terminals are not for connection to conventional TV sets.

INTERFACE CONNECTOR (D-SUB 15 pin)
Used for serial interface connection to a computer or controller.



EXT SYNC IN terminals (BNC jacks)
One of these terminals is used for inputting an external sync signal from a sync generator, and the other is used for loop through when the player is operated in the EXT SYNC MODE. When the external sync signal is present at the input, the player enters the EXT SYNC MODE automatically.
*Input condition: [75Ω, MIN: 0 ~ −3V, MAX: +1 ~ −5V, Negative]

GEN SYNC OUT terminal (BNC jack)
To externally synchronize another player with the composite sync of this LaserVision player, connect this terminal to one of the EXT SYNC IN terminals of the player.

DIGITAL/ANALOG AUDIO OUT terminals (RCA jacks)
These terminals output LaserVision Disc audio (analog) and the audio for LaserVision with Digital Sound Discs.
Connect these terminals to the CD or AUX input terminals etc. of your stereo amplifier. Do not connect them to your amplifier PHONO input.

ANALOG AUDIO OUT terminals (RCA jacks)
These terminals output the analog audio of LaserVision Discs only. Connect them to the AUX input terminals of your stereo amplifier. Do not connect these terminals to your amplifier PHONO input.
These terminals do not output the digital sound from LaserVision with Digital Sound Discs.

REAR PANEL FACILITIES

ABOUT THE AUDIO OUTPUT TERMINALS

This player is equipped with two sets of audio output terminals.
As shown in the table below, the DIGITAL/ANALOG terminals are able to output all the audio signals that can be played back by the player.

Type of Disc	Playback Sound	Output Terminals	
LaserVision with Digital Sound Discs (Discs with the mark)	Digital	DIGITAL/ ANALOG	Can be selected with the AUTO
	Analog	DIGITAL/ ANALOG, ANALOG	
LaserVision (Discs without the mark)	Analog	DIGITAL/ANALOG, ANALOG	

For ordinary operation, connect the DIGITAL/ ANALOG terminals to your amplifier.
The ANALOG terminals are provided for developmental use. They do not need to be used for ordinary operation.

12. SPECIFICATIONS

1. General

System and Disc spec. . . LaserVision Videodisc System
*1 Maximum playing time. . . . .
12-inch standard play disc: 30 min/side
12-inch extended play disc: 60 min/side
8-inch standard play disc: 14 min/side
8-inch extended play disc: 20 min/side
Spindle motor speed
Standard play disc . . . . 1,800 RPM
Extended play disc . . . . . . 1,800 RPM (inner circumference)
to 600 RPM (outer circumference)
[When using 12-inch disc]
Power requirements . . . . . 120 V AC, 50/60 Hz
Max. power consumption . . . . 100 W
Dimensions . 420 (W) × 453 (D) × 140 (H) mm
16-17/32 (W) 17-27/32 (D) X 5-1/2 (H) in
Net weight (without package) . 14.7 kg (32.4 lb)
Operating temperature . . . . +5 to +35°C (+41 to 95°F)
Operating humidity . . . . 5 to 90 %
(There should be no condensation.)

2. Video characteristics (two systems)

Format . . . . NTSC color system
Video output
Level . . . . . . 1 Vp-p nominal, sync. negative, terminated
Impedance . . . . 75Ω unbalanced
Terminal . . . . RCA jack

3. Audio characteristics

DIGITAL/ANALOG terminals
Level . . . . 2 Vrms (0 dB)
Impedance . . . . 1 kΩ less
ANALOG terminals
Level . . . . . 500m Vrms (1 kHz 100 % mod.)
Impedance . . . . 2 kΩ less
Terminal . . . . Both RCA jacks
Number of channel 2

4. External Synchronization

Sync. input (two systems)
Level . . 3 Vp-p or more and less than 6 Vp-p
Impedance . . . . 10 kΩ less
Terminal . . . . BNC jack
Sync. Gen. output
Impedance . . . . 75 Ω
Terminal . . . . BNC jack

5. Other Terminals

EXT CONT (front panel) . . Miniature phone jack
INTERFACE CONNECTOR . . . . . 15 pin, D-SUB connector (rear panel)

6. Furnished accessories

Audio connecting cord with RCA-plugs (1.5m) 1
Video connecting cord with RCA-plugs (1.5m) 1
Operating instructions 1

7. Functions

	CAV	CLV
Play (Normal play mode with sound)	YES	YES

8. Functions with the optional remote control unit

	CAV	CLV
Play (Normal play mode with sound)	YES	YES
Stop	YES	YES
Step forward/reverse	YES	YES*2
Multi-speed play forward/reverse	YES	YES*2
Multi-speed set	YES	YES
Scan forward/reverse	YES	YES
Frame number search	YES	YES
Time number search	NO	YES
Chapter number search	YES	YES
Auto stop	YES	YES
Frame number display	YES	YES
Elapsed time number display	NO	YES
Chapter number display	YES	YES
User programing and program play	YES	YES

NOTES:
Specifications and design subject to possible modifications without notice, due to improvements.
**1 Actual playback time differs for each disc.*
**2 On some CLV discs on which a second code is not recorded, the picture cannot be advanced forward or reverse frame-by-frame neither is multi-speed play possible.*

PIONEER
The future of sound and vision.

Service Manual

SERVICE GUIDE

ORDER NO.
ARP 1759

LASERVISION PLAYER

LD-V8000

CONTENTS

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FI APR. 1989 Printed in Japan

1. MAJOR FEATURES OF LD-V8000

- **High-speed Search**

A dual-shaft horizontal support linear motor is used in the pickup drive mechanism to enable high-speed access of the pickup. In addition, a servo control employing a digital servo IC and 16-bit MAIN CPU makes high-speed search operation possible.

- **Digital TBC and 1-frame Video Memory**

After the video signal is converted into a digital signal using an A/D converter with a sampling frequency of about 14 MHz (4fsc) and 8-bit quantization, time axis correction is performed by the TBC (time base corrector) using the line memory. Furthermore, since a video memory in which 1 frame (2 fields) of image data can be stored (with a memory capacity of 4 Mbits) is incorporated, the picture just before the search operation is activated is stored in memory to be output during the search, so that "seamless search" is possible.

- **External Synchronization with Vertical/Horizontal Lock**

By locking the built-in sync generator with the external sync signal, the vertical and horizontal frequencies can be synchronized externally .

- **An RS-232C interface is provided as standard for external control.**
- **A digital audio playback function is provided.**

2. P.C. BOARDS USED IN THE LD-V8000

2.1 MAJOR PC BOARDS USED IN THE LD-V8000

- **DSCO (Digital Servo & Control)**

This includes the system control circuits centered around the 16-bit CPU μPD70320 and the servo IC PD2021 for controlling FTS and SPDL.
PD2021 is a digital servo IC developed exclusively for the LD-V8000 and incorporates the A/D, D/A converters and the Digital Servo processor.

- **DEGE (Decoder & Generator)**

This includes PA5010 for video signal processing and PA0034A for analog audio signal processing, to perform the same analog signal processing operations as in conventional LD players.
It also incorporates the Reference Sync Generator IC HD440072. The output of this sync generator IC is locked to the external sync signal and outputs the required reference signals to each section when an external sync signal is input. Since the LD-V8000 has external synchronization functions including H-V lock but is not provided with the burst lock provided in LD-V6000 series models, its circuit is simplified when compared with that of LD-V6000 series models.

- **DTMC (Digital TBC & Memory Control)**

This includes the digital TBC and two ICs (PDB005 and PDB006) which control the 2-field/1-frame video memory.
All the digital signal processing of the video signal is performed on this board.

- **DADB (Digital Audio Board)**

This section performs signal processing of the digital audio signals and does not use special ICs.

Among the functions of the above PC boards, circuit operations of the following functions which are used for the first time in the LD-V8000 are described in this Service Manual:

- ○ Focus, TRKG (tracking), Slider and SPDL (spindle) servo based on the Digital Servo IC PD2021
- ○ Digital TBC and video memory control
- ○ System control circuits

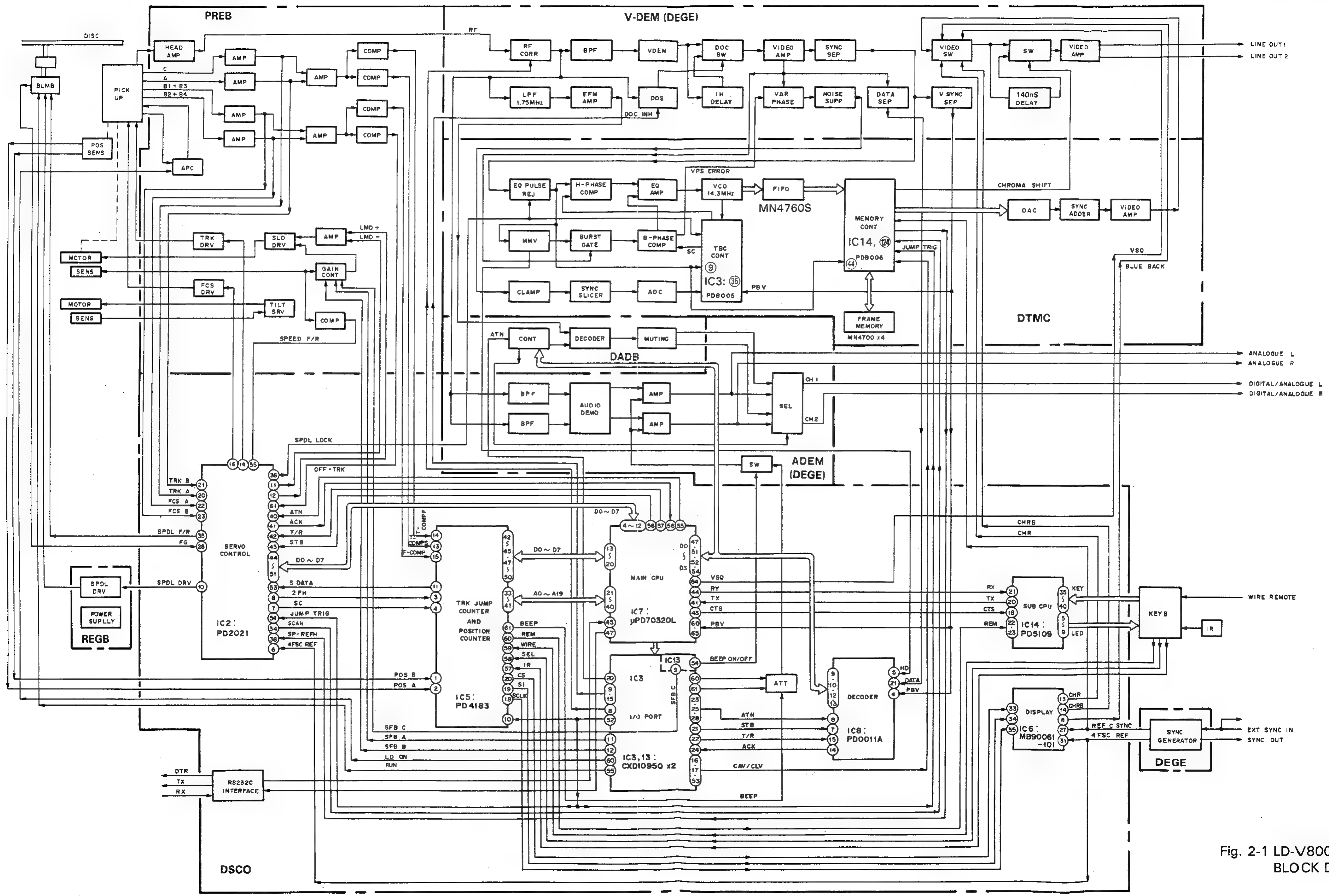


Fig. 2-1 LD-V8000
BLOCK DIAGRAM

3. VIDEO SIGNAL PROCESSING AND DIGITAL TBC

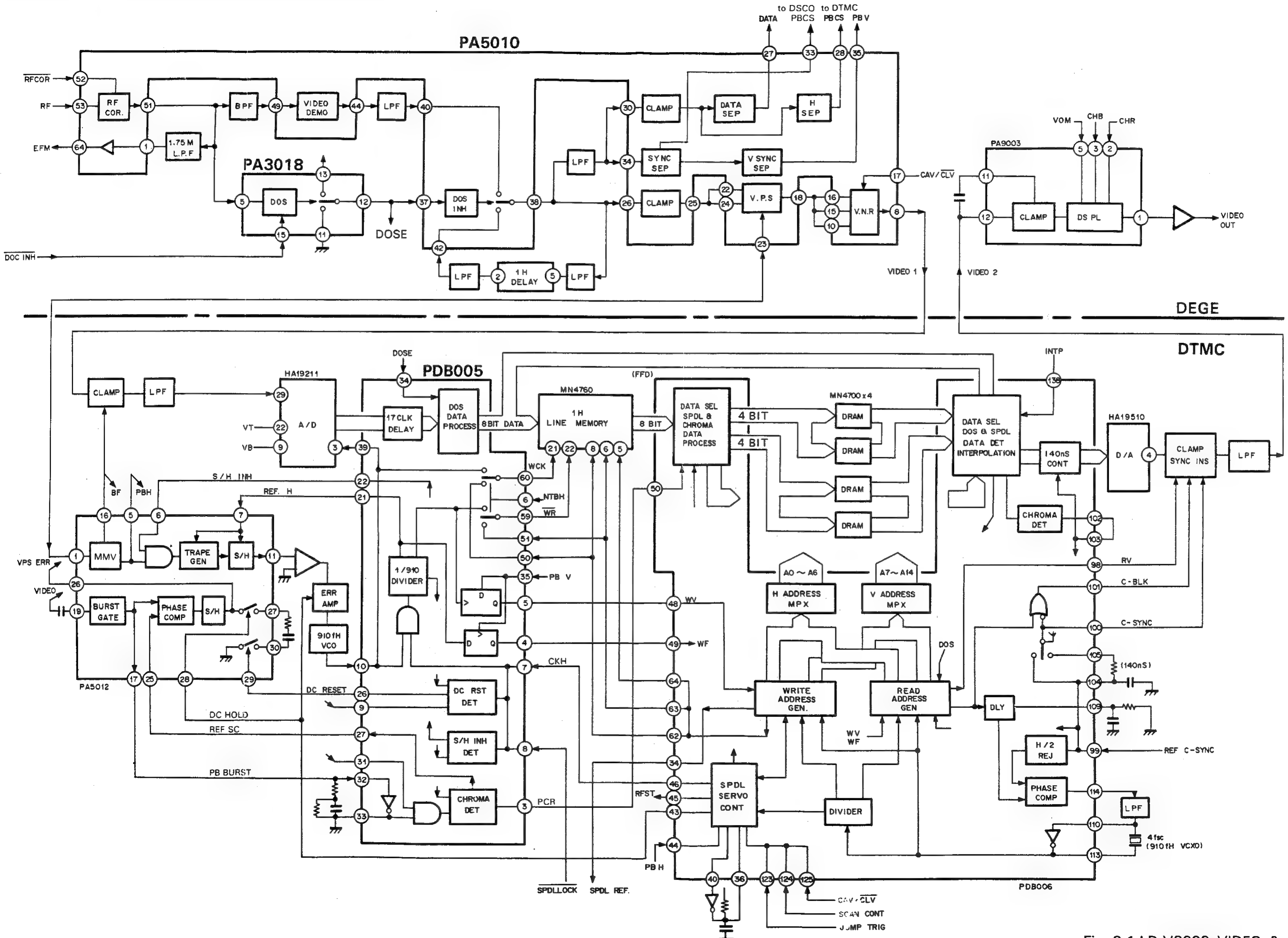


Fig. 3-1 LD-V8000 VIDEO & DIGITAL TBC BLOCK DIAGRAM

3.1 OUTLINE

The video signal processing circuits in the LD-V8000 are divided into two PC boards; DEGE and DTMC. The DEGE board includes the video processing section based on video IC PA5010, the demodulator section, the sync separator section, and the analog signal processing section including the VPS and VNR, etc.
On the DTMC board, the video signal from the DEGE board is converted into a digital signal by the A/D converter, and then the signal is returned to an analog signal by the D/A converter after being controlled by the Digital TBC and 2-field video memory, to be supplied to the DEGE board again. In other words, the DTMC board includes all the video signal digital processing sections.
The figure is a block diagram of the entire video signal processing section (Fig. 3-1) on the two boards.
In this diagram, the upper half around the PA5010 is on the DEGE board while the lower half around PDB005 and PDB006 are on the DTMC board.
The signal processing in PA5010 is performed in almost the same way in conventional LD players which have no DTBC or video memory, as shown in the block diagram. The differences in this section from that of LD players like the CLD-3030/1030 are the use of PA3018 for the detection of DOS and the absence of a CCD element.
The video signal from pin 8 of PA5010 is input to the DTMC board from the DEGE board as the VIDEO 1 signal. Since the time base of this video signal is not corrected by a CCD element, it contains jitter and eccentricity components.
After data is written to the line memory using a clock following the above jitter components, data is read out using the reference clock from the crystal oscillator so that time base correction is possible. This principle is the same as the function of the RAM used in the signal processing section of a CD player.
To generate the clock following the jitter components, PA5012 detects time base error components which are used to control the 910fH VCO. The VCO output is divided in PDB005, and the reference signals (REFSC, REFH) for error detection and the write start timing signal ($\overline{WR}$) to line memory are output. Also the signals to hold errors from PA5012 when unlocking the SPDL signal or shifting the reference signal, etc. and the signal to hold the VCO frequency are supplied from PDB005 to PA5012. (DC RST, DC HOLD, S/H INH)
In PDB005, when it is recognized that dropout has been corrected in the data from the A/D converter by the 1H CCD, from the DOSE signal input to pin 34, identification data is inserted at the LSB of the 8-bit data, then output to the line memory. (DOS DATA Process Block)
Data is read from the line memory using the 910fH VCXO signal which is locked to C-SYNC from the Sync Generator IC (HD440072) as the reference clock, in the same way as when writing and reading the field memory.
Since this reference clock is used as the master clock of PDB006, the operation up to writing to the line memory is performed using the VCO clock, and operations after reading out are performed using the VCXO clock.
In PDB006, after the data based on the PCR signal of the burst phase judgment data input to pin 50 from pin 3 of PDB005 is added to the data from the line memory, the signal is divided into two parts; the upper 4 bits and lower 4 bits, which are then output to four RAMs. PDB006 also controls the data write and read addresses of the four RAMs (2 field memories), as well as the dropout correction and special effects processing.
In the LD-V8000, most of the spindle servo section is included in the Digital Servo Processor PD2021. To do this, the SPDL REF signal which is synchronized with the D-RAM write address is input to PD2021 as the SPDL REFH signal. And when performing scanning and jump operations, the CKH or DC HOLD signals are output to perform reference shift. When reference shift is performed, the commands to execute reference shift for the spindle servo are supplied from PDB006 to PD2021 via the main CPU.
In the Still mode with a CLV (Constant Linear Velocity) disc, the line memory is used as a 1H delay line, so as to generate the data to be used for interpolation according to the relative level of the luminance signals of the two scanning lines; this is output to the field that is next to the normal output from the field memory, to breduce line flickering.
Moreover, the burst phase judgement data which is inserted before it is written into the field memory is used to check the continuity of the burst phase in the video signal that is output to the D/A converter, andif required, the signal is shifted by 140 nsec. All these sections are included in IC PDB006.
Summarizing the above description, PDB005is operated with the clock following the jitter or eccentricity components included in the video signal input from the DEGE board, while PDB006 is operated with the clock synchronized with the REF C-SYNC signal. The line memory performs the data transfer between PDB005 and PDB006. In other words, PDB005 and PDB006 are connected via the line memory, and all these operations are performed using a digital TBC. The spindle servo should be locked before any operation of the digital TBC. The chief functions of PDB005 and PDB006 are as follows (block names are as shown in the block diagram):

- **PDB005**
  - ○ Line memory write clock generation and VCO loop control
    (1/910 divider, DC RST Detection, S/H INH Detection)
  - ○ Insertion of DOS data into the video data for the color DOC (17 clock delay, DOS data processing)
  - ○ Chroma polarity and judgment of field of the playback video signal (Chroma Detection)

• PDB006

- Line memory read-out and video memory write/read control
  (Write/read address control, DATA SEL, H/V Address MPX)
- Color DOC (DOS DATA Detection)
- 140 ns shift control (Chroma detection, 140 ns control)
- Generation of clock synchronized with REF C-SYNC (H/2 REJ, PHASE COMP, Divider)
- Reference shift control of DIGITAL TBC loop (SPDL Servo Control)

The above functions are described on the following pages.

3.2 DIGITAL TBC

• Functions of Line Memory and Relationship with SPDL Servo

The line memory uses FIFO (First In - First Out) operation and does not have an address input unlike normal memory ICs. The data reading starts from the data which was written first.
For this, independent address counters are provided for writing and reading, and the $\overline{WR}$ and $\overline{RD}$ signals are the reset signals for the two address counters. The WCK and RCK signals are the clocks of the two counters. (See Fig. 3-2.)

INTERNAL BLOCK OF MEMORY

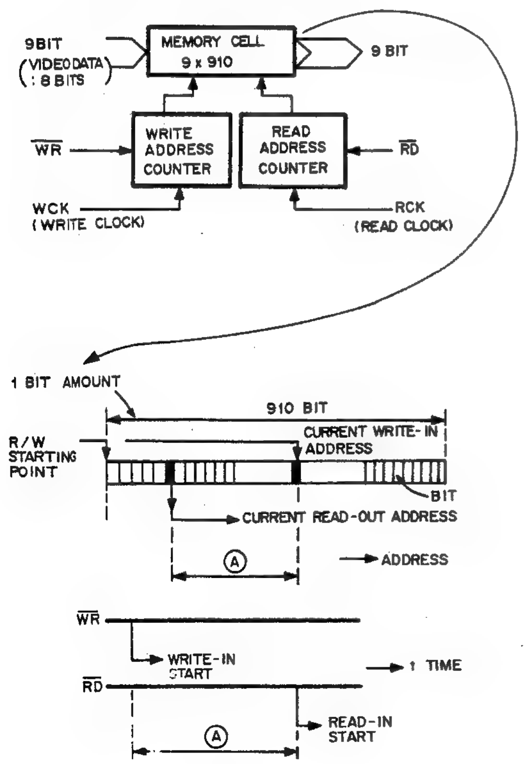


Fig. 3-2

Therefore, when the $\overline{WR}$ signal goes low, the Write Address Counter is reset, then the data is written to the memory sequentially according to the counting up of the counter. Then, when the $\overline{RD}$ signal goes low, in the same way, the Read Address Counter is reset, then the data is read out sequentially from the data which was written first according to the counting up of the counter.
As a result, as long as the $\overline{WR}$ signal is before the $\overline{RD}$ signal, the written data is read out with a time delay which is the difference between $\overline{WR}$ and $\overline{RD}$ (Fig. 3-2 Ⓐ). The maximum delay period is determined by the capacity of the line memory: Since MN4760 has a 910-sample memory, the delay time is 910 addresses = 1H.

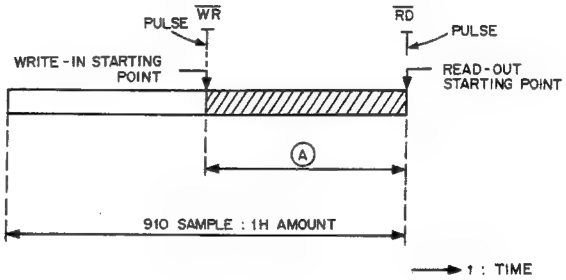


Fig. 3-3

The above diagram is made by modifying the diagram on the previous section so that the read start point is at the right end.
As the data supplied to the line memory is the A/D-converted video signal, both $\overline{WR}$ and $\overline{RD}$ signals go low every 910 samples, i.e., in every 1H period.
Since the $\overline{RD}$ signal is formed from the signal produced by dividing the 4fsc VCXO signal by 910, the period of the $\overline{RD}$ signal is fixed and thus the read-out timing is also fixed. Further, when the $\overline{WR}$ signal is locked to the PBH signal, the length of Ⓐ in the above diagram varies within the difference between the $\overline{RD}$ period and the PBH period. If the PBH period is longer than $\overline{RD}$, since the write timing is slower than the read timing, the period Ⓐ will be shorter, and when $\overline{WR}$ and $\overline{RD}$ are matched, read data will be lost. In this condition, the speed of the spindle motor is slower than the regular speed.
When the speed of the spindle motor is faster, since the PBH period, that is, the $\overline{WR}$ period, is shorter than the $\overline{RD}$ period, the length Ⓐ will be longer, and the end of the data will overflow from memory.
Therefore, if the speed of the spindle motor is controlled so that the period Ⓐis maintained at a fixed length, the data will not overflow nor be lacking. To do this, the PBH signal is locked to the $\overline{RD}$ signal; this is the same spindle servo function as in conventional models.
However, eccentricity or jitter components cannot be absorbed by the spindle servo on its own, the write start point, that is, the $\overline{WR}$ point, may fluctuate to the left and right.

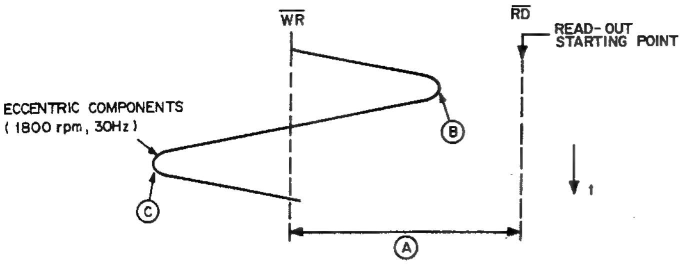


Fig. 3-4

Even when the $\overline{WR}$ point fluctuates to the left and right, data read-out is possible without overflow or lack of data from the line memory unless the eccentricity components exceed the length Ⓐin Fig. 3-4. In other words, the line memory functions as a variable delay line to absorb eccentricity components in the same way as the conventional CCD. The difference with the CCD is that there is no signal deterioration due to fluctuations of the CCD clock since digital signal processing is performed using A/D converted data.
Actually, since the spindle servo functions so that the period Ⓐ in Fig. 3-4 is separated by about 1/2H, eccentricity components of approx. ± 30 μs can be absorbed by the line memory and time axis correction is made possible.

- **A/D Conversion Timing**

Since the PBH period is longer than the REFH period at point (B) in Fig. 3-4, the 1H period is longer than usual, and is shorter at point (C). (See Fig. 3-5.)

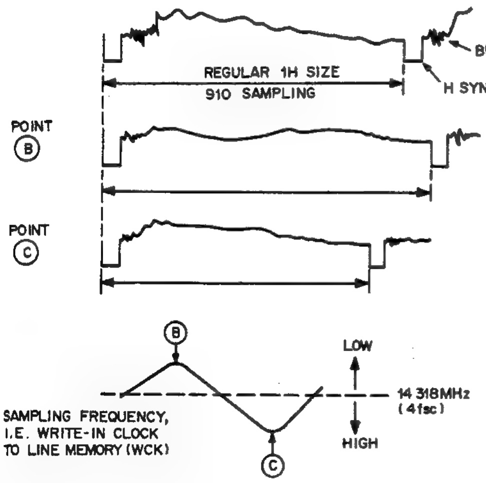


Fig. 3-5

Even when the length of the 1H period varies, the number of samples for the A/D conversion of 1H should be 910. Therefore, the clock frequency of A/D conversion should be varied according to eccentricity components.
This A/D conversion clock is used as the clock of the address counter for line memory.
And since VPS processing of the video signal is performed before A/D conversion, the REFSC signal for VPS error detection should vary according to the eccentricity components. For this, the VPS error is detected by comparing the burst signal using 1/4 of the clock frequency of A/D conversion.

3.3 OPERATION OF PDB005

- **Write Clock Generation**

To generate the clock frequency which varies according to eccentricity components, PDB005 and PA5012 form a loop which controls the 910fH VCO. (See the block diagram.)
The output of the 910fH VCO is input to pin 10 of PDB005, and output as the REF H signal. When this REF H signal is input to pin 7 of PA5012, the trapezoidal signal for error detection goes up, synchronized with the falling edge of REF H, and is sample/hold at the falling edge of the PBH signal to detect the H rate error. (See Fig. 3-6.)

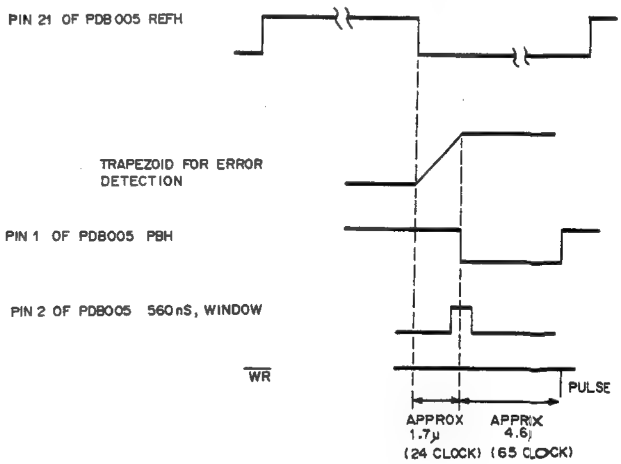


Fig. 3-6

- **VCO Loop Control**

To detect the lock condition of the 910fH VCO consisting of PA5012 and PDB005, whether the falling edge of PBH is within the width of the 560 ns pulse for position detection is checked inside PDB005. This 560 ns pulse is made by dividing the VCO output, and is positioned approx. 1.4 μs (20 clock pluses) away from the falling edge of REF H. This detection pulse is output from pin 2 of PDB005, and input to the DC RESET DET section via pin 1.

In the DC RESET DET section shown in the following figure, the output of the latch will be "L" when the position of PBH is moved because the detection pulse is latched at the initial point.

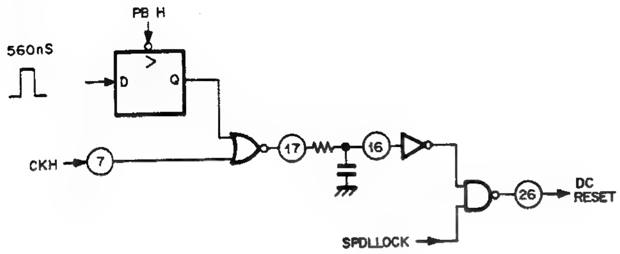


Fig. 3-7

When the latch output goes low, pin 17 is inverted from low to high, and after the time constant of pins 17 and 16, pin 26 DC RESET goes high. The switch of pin 30 inside PA5012 is turned ON by this and the burst error is reset to "0". Therefore, the VCO loop is controlled by only the H error signal, and the falling edge of PBH comes to the center of the 560 ns pulse. (This is because the inclination of the trapezoidul signal is adjusted so that the PBH comes to the center of the 560 ns pulse when the burst error is "0".)
When the spindle servo is not locked or reference shift is performed (when pin 7 CKH is at high level), DC RESET goes high to reset the burst error.
Also the DC HOLD signal, used to hold the burst error,is input to the burst error detection section of PA5012 from pin 43 of PDB006, so that the write start point (WR phase) of the line memory is not shifted after it is once locked, in the following cases:

1. When CKH is at high level.
2. When the phase difference between WR and RD of the line memory increases too much.

The S/H INH signal is input from Pin 22 of PDB005 to the H-error detection section of PA5012, so that the sample & hold of the error signal is inhibited when necessary.
While the CKH input to pin 7 of PDB005 is at high level, that is, when reference shift is being performed, since the REF H signal is held in the same way as in previous models, S/H INH goes low when the SPDL signal is not locked. And after the H-error detection trapezoid signal starts, when dropout is detected before the PBH signal is inverted to low, the S/H INH signal goes low since errors in the original PBH are not processed by the sample & hold circuitry.

Summary of S/H INH, DC HOLD and DC RESET

	When SPDL is unlocked	CKH = H
S/H INT	L (ON)	L
DC HOLD	L	H (ON)
DC RESET	H (ON)	L

- **Other Function Blocks in PDB005**
- **CHROMA DET (CHROMA DETECTOR) SECTION**

The PB burst signal is picked up from the PB burst signal from pin 32 and BF (burst flag) signal from pin 31, and is compared with the signal which consists of the VCO output divided by four, to detect the burst signal phase in each 1H period.
The REF SC supplied to PA5012 is inverted in every 1H period so that its relationship with the phase of the detected PB burst signal is kept constant.
The result of PB burst signal detection is output from pin 3 and input to pin 50 of PDB006 as the PCR (play chroma) signal.

- **WV, WF SIGNAL GENERATION**

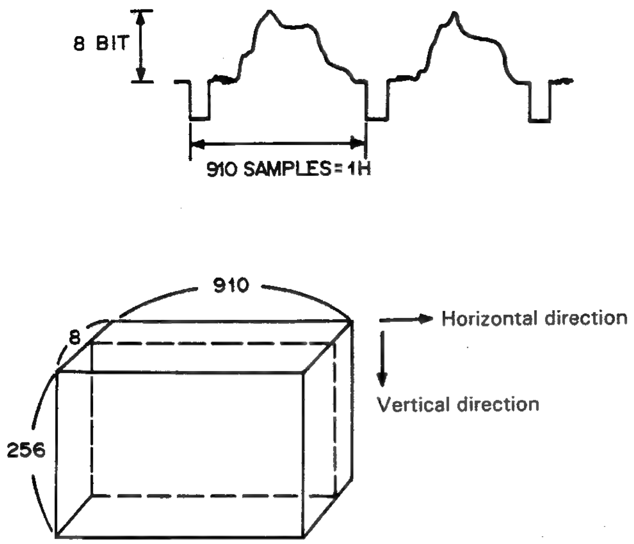
WV: The signal that the PBV signal input from pin 35 is latched by WR.
This signal is input to pin 48 of PDB006 and used to indicate the first vertical address of the field memory.

WF: The signal that the REF H is latched by PBV.
It indicates that the video data written in the field memory is either the first field or the second field, and is input to pin 49 of PDB006.
In PDB006, since reading out from the field memory is synchronized with C-SYNC from the sync generator, it is not synchronized with the write sync (PBV, PBH signal.)
Therefore, when reading data from the field memory, it is necessary to detect whether the data is from the 1st field or 2nd field before.

3.4 FUNCTIONS AND OPERATIONS OF PDB006

- **Line Memory Reading and Video Memory Control**

The video data read out from the line memory is divided into two, the upper 4 bits and the lower 4 bits, which are stored in the video memory (MN4700) as they are. Therefore, the read timing (RD signal) from the line memory should be synchronized with the timing of writing to the video memory.
The timing of writing to the video memory, that is, the RAM writing addresses, are generated by the Write Address Generator in PDB006. For this, the RD signal to the line memory is also generated in the same block. And since the RD signal should be synchronized with the REF H signal for SPDL servo, the SPDL REF signal which is supplied from pin 34 of PDB006 to the servo IC PD2021 is also generated in the same block.
The 1-field data written to the video memory is as shown shown in the following diagram.



Total data for 1 field (910 × 256 × 8 = 1863680 (bits)

Fig. 3-8

In the LD-V8000, since four 1Mbit DRAMs (MN4700) are used, image data for 2 fields can be stored in memory. The 8-bit data is divided into two; the upper and lower 4 bits, and written into the 2 DRAMs.
Since the DRAM has 256 = 2^8 vertical addresses, part of V-SYNC is not stored in memory in the same way as in conventional LD players with a video memory (LD-S1, CLD-3030).
As MN4700 incorporates an 8-bit shift register for each data bus, the input data is processed in 8-bit units. However, since there are 910 samples in the horizontal direction, 910/8 = 113 gives a surplus of 6, so data for 6 samples is ommitted.
To do this, horizontal addresses from 0 to 112 are set, and the address counter is stopped so that the remaining 6 samples are not stored in memory. (See Fig. 3-9.)

HORIZONTAL AND VERTICAL ADDRESSES AND ACTUAL VIDEO SIGNAL

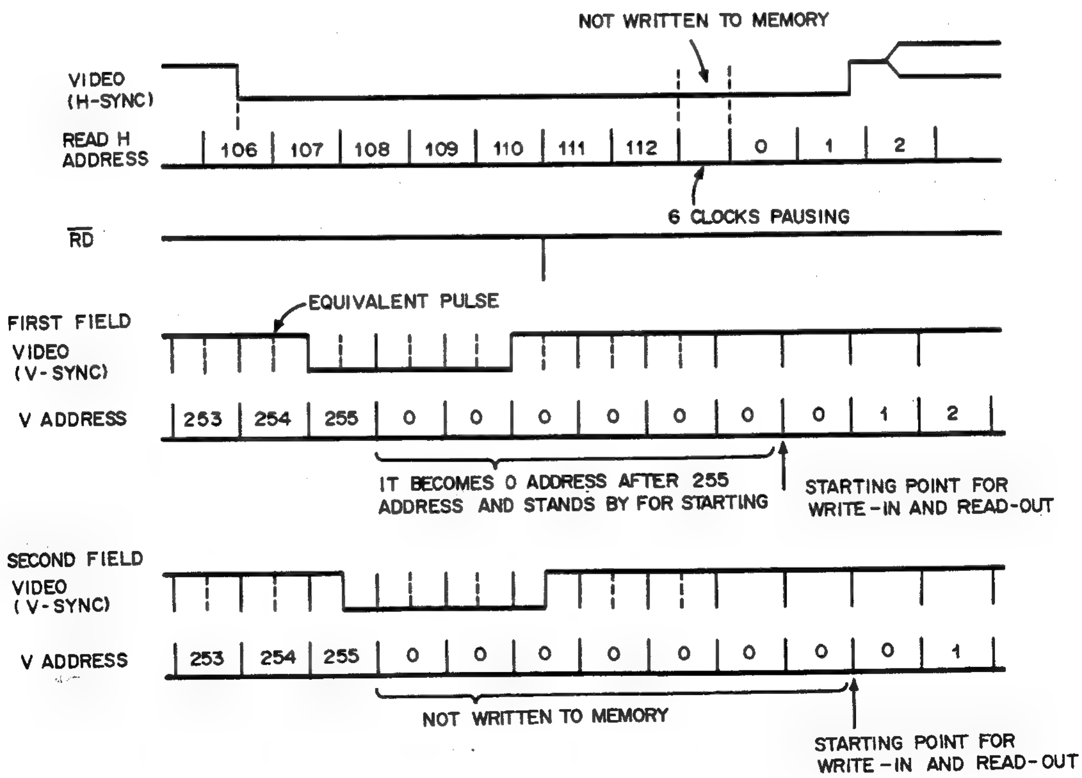


Fig. 3-9

The generation of DRAM write addresses is performed in the Write Address Generator section in PDB006. Since the start of the address is triggered at pin 48 of PDB006 by the WV signal which is output from pin 5 of PDB005 to pin 48 of PDB006, writing into DRAM is actually performed synchronized with the PBV signal.
The read address of the DRAM is generated by the Read Address Generator section, and is triggered by the REF C-SYNC signal which is input from the Sync Generator IC to pin 99 of PDB006.
The clock used by these two address generators consitsts of the 4fsc = 910fH clock devided by eight which is synchronized with the REF C-SYNC signal. And since the read clock for the line memory is the 910fH clock before division, the same clock frequency is used to control all the operations after reading out from the line memory. This is because PDB006 performs all operations using the 910fH clock.

• 910fH VCXO Control of PDB006

PDB006 operates using the 910fH VCXO output which is synchronized with the REF C-SYNC signal input to pin 99 from the SYNC GEN IC (DEGE IC4: HD440072) as a master clock. The result of the phase comparison between the internal H-SYNC, which is synchronized with the horizontal address counter of the field memory, with the signal, which the REF C-SYNC signal is half H rejected, is output from pin 114 of PDB006. Since this output signal controls the 910fH VCXO via an externally-connected LPF (low-pass filter), the VCXOoutput is locked to the REF C-SYNC signal.
Since the time constant connected to pin 109 is set to the delay time of the internal H SYNC, when it is varied, the phase of the REF C-SYNC signal to be inserted in the H address for reading the field memory and the read-out data will be varied.

• Chroma Judgment and 140 ns Shift Operation in PDB006

The PCR signal input to pin 50 of PDB006 is inserted at the LSB of the video data as the horizontal address 1 to be written into the field memory. This data is used to judge the continuity of the chroma (burst) phase when the data is read out from the field memory.
The result of the non-continuity/continuity judgment is output from pin 102 as the CRM INV signal, and input to pin 103 as it is. To maintain the continuity of the burst phase, the video data output to the D/A converter is delayed by 2 clock periods (140 ns).
Since the C-SYNC output from pin 100 is delayed by the time constant connected between pins 104 and 105 (140 ns), when the video data is delayed by 140 ns, the SYNC signal will also be delayed.

• Dropout Compensation (Function of PDB005 + PDB006)

The detection of dropout is performed by PA3018 and correction is performed by replacing the dropout with the delayed CCD output.
In this system, color DOC operation is performed; the B/W 1H delay video signal inserted in the dropout section is replaced by the video data of about 2H before.
First, the DOS signal from pin 12 of PA3018 is input to pin 39 of PDB005 as the DOSE signal. In the PDB005, when the DOSE signal goes high, the lower 2 bits of the video data to be written into the line memory are set to "1" for more than 4 clock pulses continuously to multiplex the video data for the DOS signal. Further, if the same pattern as the DOS signal is present in the normal video data, the LSB is set to "0" forcibly to prevent mis-detection.
This DOS data is written to the field memory as it is.
When the DOS data is detected in reading out from the field memory, the data of 6 horizontal addresses (= 48 clock pulses) is replaced by the video data 2H before to perform color DOC.
Actually, to detect the DOS data (pattern) in the video data and replace it with the data 2H before, it takes a certain time to change the vertical address of the field memory and to read the data 2H before. Therefore, the DOS data should be inserted the above period prior to the actual dropout section. For this, the video data from the A/D converter is delayed by 17 clock pulses, then the insertion of the DOS data is performed so that the DOS data is inserted in the position 17 clock pulses before the dropout portion.

• Operation of Spindle Servo Control Section

When the reference shift is performed during scanning or jumping with a CLV disc, writing data to the video memory is suspended during this period.
At the same time, the RFST signal at pin 45 of PDB006 goes high to signal to the main CPU that reference shift has been performed. At this time, the SPDL REF is also shifted. The main CPU outputs a command to PD2021 to perform reference shift, and the spindle servo functions so that the edges of the SPDL REF signal and the PBH signal are matched.
The spindle servo functions to control the disc rotation, that is, the period of the $\overline{\text{WR}}$ signal, so that the difference between the $\overline{\text{RD}}$ signal and the $\overline{\text{WR}}$ signal is kept within approx. 30 μs.
But when there is excessive eccentricity or scanning operation, the relationship between the $\overline{\text{RD}}$ signal and the $\overline{\text{WR}}$ signal becomes disordered, and the data cannot be read out from the line memory. Therefore, to check the positions of both the $\overline{\text{RD}}$ and $\overline{\text{WR}}$ signals, the position of the pulses corresponding to the address between 98 and 105 and between 102 and 105 in the horizontal address and the position of the falling edge of the PBH signals are continuously monitored, as shown in Fig. 3-10.

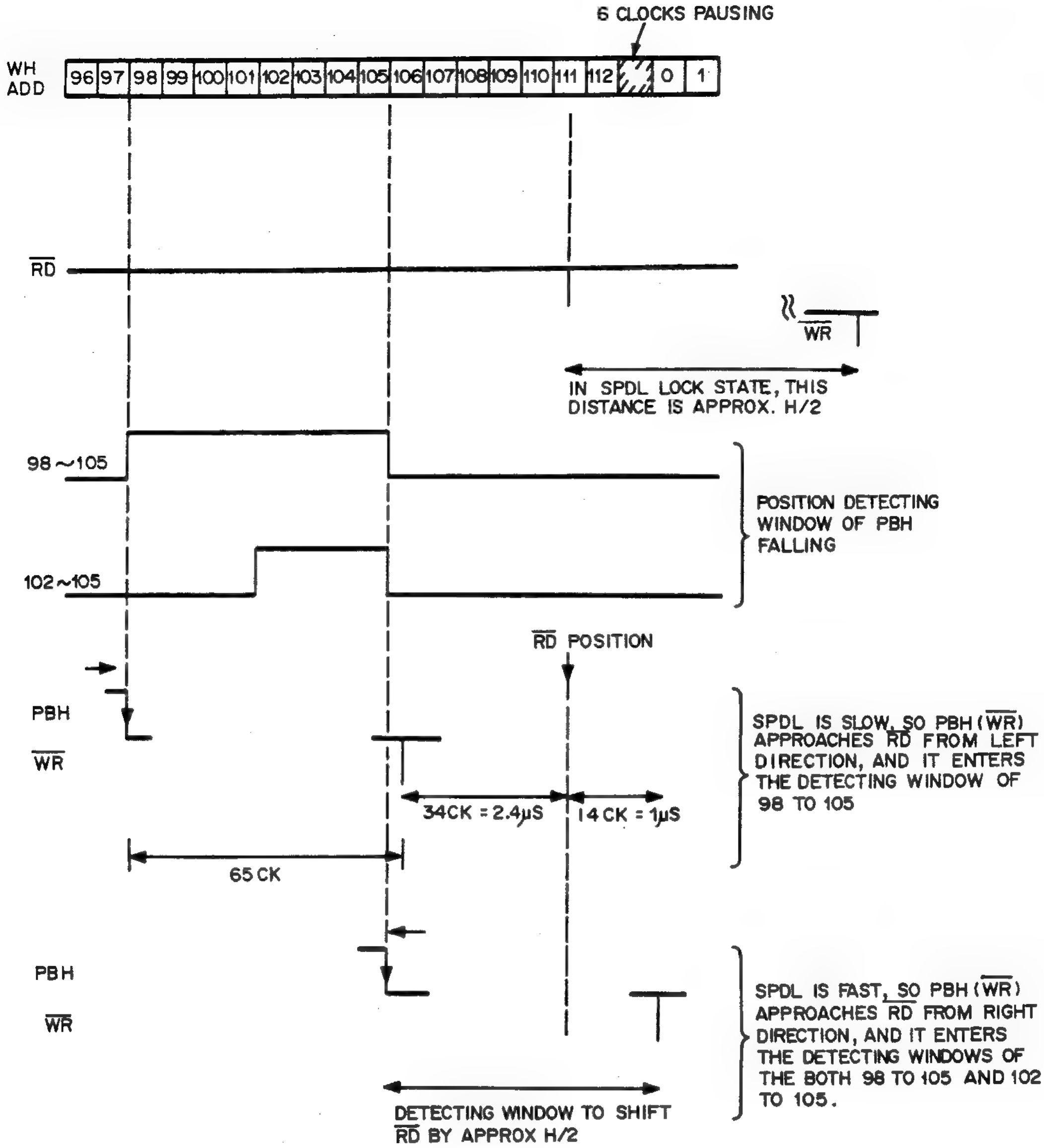


Fig. 3-10 Timing and Detection when the Spindle Motor is Fast and Slow

The signal processing when the speed of the spindle motor is faster than normal and when it is slower than normal are described below:

- **WHEN THE SPINDLE MOTOR IS SLOW:**

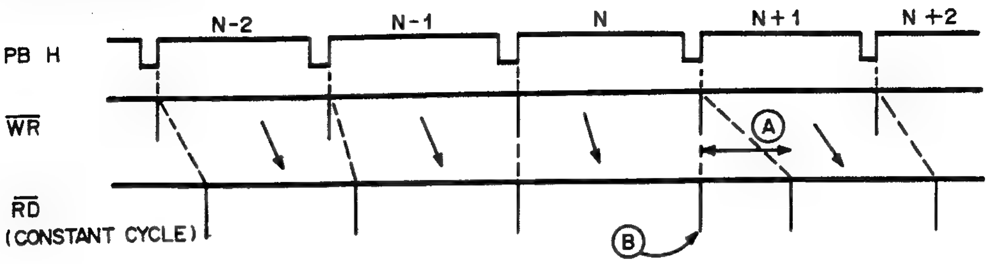
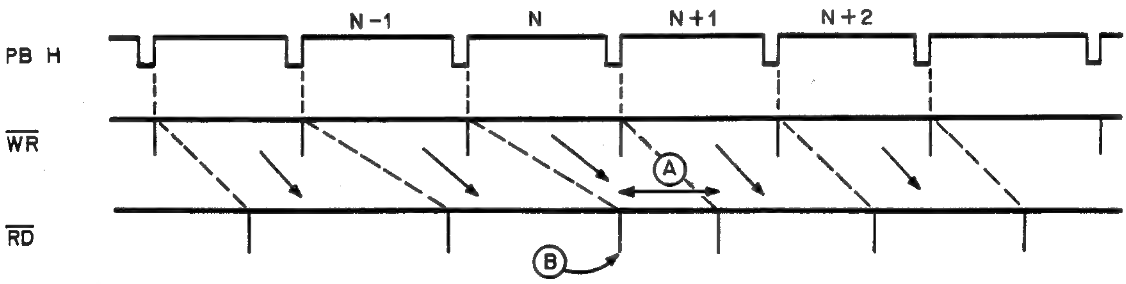


Fig. 3-11

In this case, since the period of the $\overline{\text{WR}}$ signal is longer than that of the $\overline{\text{RD}}$ signal, the $\overline{\text{WR}}$ signal becomes closer to the $\overline{\text{RD}}$ signal from the left side. If this condition continues as it is, the $\overline{\text{RD}}$ signal will pass the $\overline{\text{WR}}$ signal and data for the same line will be read out twice. Becaue of this, when the falling edge of the PBH signal comes to the detection window of address 98 — 105, address 56 is loaded as the initial value of the next H address counter (to count from 0 to 112). Then the subsequent $\overline{\text{RD}}$ signal (corresponding to an H address of 111) comes to the position separated by 1/2H period (period Ⓐin the above diagram), as shown in Fig. 3-11.
Therefore, the data on the (N + 1) line is read out by the $\overline{\text{RD}}$ signal at point Ⓑ, and read again for a 1H period from the beginning by the next $\overline{\text{RD}}$ signal which is at the position separated by period Ⓐfrom point Ⓑ. By this operation, the relationship between the $\overline{\text{WR}}$ position and the $\overline{\text{RD}}$ position is resumed by shifting the $\overline{\text{RD}}$ signal by a 1/2H period.
Since writing to the line memory is always performed continuously, the data will not be lost and there is no affect on the screen even if the $\overline{\text{RD}}$ signal is shifted by 1/2H.
Since the data read out from the line memory is immediately written into the field memory, the writing to the field memory is inhibited during period Ⓐshown in Fig. 3-11.

- **WHEN THE SPINDLE MOTOR IS FAST:**



In this case, since the $\overline{\text{WR}}$ period is shorter than the $\overline{\text{RD}}$ signal, the $\overline{\text{WR}}$ signal comes closer to the $\overline{\text{RD}}$ signal from the right side. If this condition continues, the $\overline{\text{WR}}$ signal passes the $\overline{\text{RD}}$ signal and the data which is not read out will be left.
When the $\overline{\text{WR}}$ signal becomes closer to the $\overline{\text{RD}}$ signal from the right side, it means that the falling edge of the PBH signal becomes closer to the detection pulse of addresses 98 — 105 and 102 — 105 from the right. When the falling edge of the PBH signal enters the two detection pulses, address 56 is loaded as the initial value of the horizontal address counter, to shift the $\overline{\text{RD}}$ signal by period Ⓐ.
However, as opposed to the operatiopn when the spindle motor is slow, if the data is read out by the $\overline{\text{RD}}$ signal separated by period Ⓐ, the data of the (N + 1)th line is read out. As a result, the Nth line data will be lost. As the data is not read out from the line memory, 1H of data in the field memory is lost.
The 1H data loss is corrected by replacing it with the data 2H before, by setting the vertical address to −2 when reading from the field memory.
For this, the LSB of horizontal address "0" the lead at the (N + 1)th line is set to "1" as data indicating that the $\overline{\text{RD}}$ signal is shifted by 1/2H, and written to the field memory.

4. SERVO SYSTEM

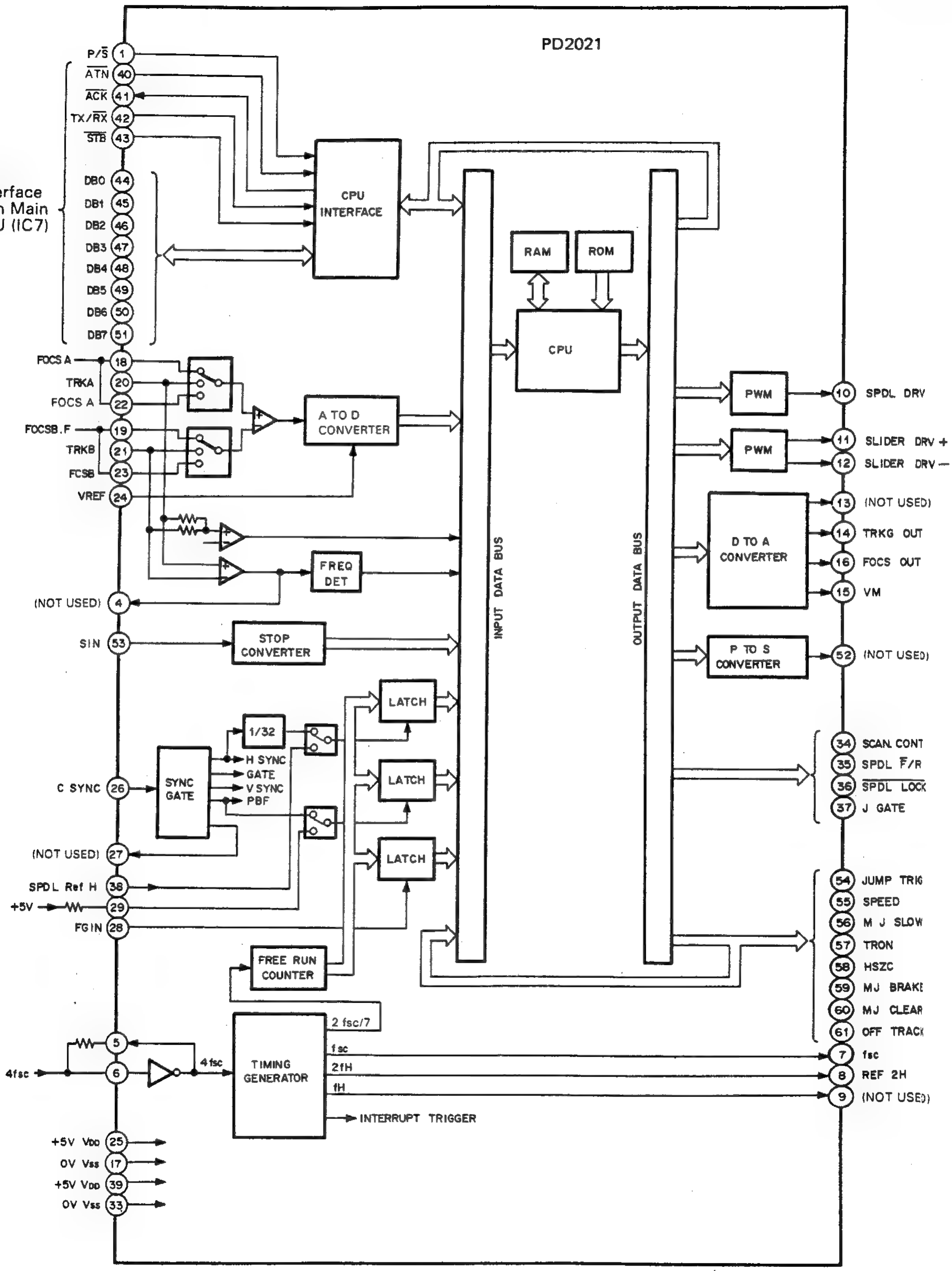


Fig. 4-1 Internal Block Diagram of PD2021

4.1 DESCRIPTION

The servo system of the LD-V8000 is based on digital servo IC PD2021, with the head amp section and the drive amp section of the FTS system on the PREB, and the spindle motor drive amp on the SYPS board.
The internal block diagram of PD2021 is shown in Fig. 4-1.
The FOCS A, B and TRKG A, B signals from the PREB are used as the FOCS error and TRKG error signals, and they are converted into digital signals by the A/D converter with a sampling frequency of 31.5 kHz and a quantization rate of 8 bits. After all the signal processing involved in focus S-shape detection, equalization, etc. have been performed, the signal is D/A converted and output as the drive signal.
For operation of the spindle servo, the periods of the FG, PBH and REF H signals are measured by a latch and free running counter, and after signal processing has been performed, the resultant signal is output from the PWM generator as the drive signal.
The interface controlling these functions in PD2021 uses the signals from pin 40 to pin 51. This bus line is connected to the exclusive I/O port of the main CPU.
The CPU incorporated in PD2021 has a high-speed multiplier which can perform high-speed numerical operations. CPUs of this type are generally called DSPs (Digital Signal Processors). In addition, the CPU in PD2021 has architecture exclusively for the servo control of an LD player.
The CPU performs the different servo processes by time-division operation, and the FOCS and TRKG signals are interrupted every 32 µs (approx.) according to A/D conversion data, while the SPDL and SLIDER signals are interrupted every 1ms (approx.).
The major difference of digital servo from conventional analog servo is that the gain and equalization characteristics are obtained by arithmetic operations in a digital filter. Therefore, since the characteristics are determined by changing the coefficient of filtering operations instead of the time constant of CR components, the required characteristics can be obtained by software, and gain setting can be done easily for different types of disc and the equalization characteristics can be easily modified according to the operation mode.
By using these characteristics in the fine control of the slider feed speed during search and tracking control, ultra high-speed search operations are possible in the LD-V8000. And focus and tracking gain adjustments are not necessary.

The main CPU outputs commands to set the operation modes and turn the various servo systems ON or OFF which are input to the servo IC, as required. The servo IC outputs the status of each servo system to the main CPU.
The detailed signal processing operations of each of the FOCS (focus), TRKG (tracking), Slider and SPDL (spindle) servo systems are described on subsequent pages.

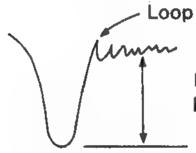
4.2 FOCUS SERVO

There are two FOCS A, B inputs from PREB to PD2021, unlike TRKG A, B. This is because two 15.7 kHz signal lines are used so that the signals are A/D converted with the same sampling frequency of 31.5 kHz as the TRKG error.
The Focus Servo block diagram is shown in Fig. 4-2.
As shown in the block diagram, the circuit configuration is completely the same as that of conventional analog servo circuits, except for the use of the A/D and D/A converters. The functions of each section are as follows:

RAMP GEN: Generates the triangular wave used to move the lens up and down.

ZERO CROSS DET: Detects the zero-cross point of the S-shaped curve of the focus error signal.

MIS LOCK DET: Judges whether the correct focus point is obtained or not, from the minimum value of the S-shaped curve.



CONTROL TIMING GEN: Determines the timing with which the loop is closed from the above two detector outputs and the level of the TRKG A + B signals.

AGC: Sets the optimum gain of the servo loop.

EQ: Performs digital filtering of the 8-bit error data. The filtering coefficient is input from the main CPU.

FOCUS MOTOR PROTECT: When the high-frequency components of the focus error signal increase, the gain is lowered by 6 dB to protect the coil.

All these functions are processed by the CPU program and arithmetic operations in PD2021. The following commands are input from the main CPU to PD2021 to control the focus servo.

- FOCUS ON
- FOCUS OFF
- FOCUS AGC ON
- FMPB ON

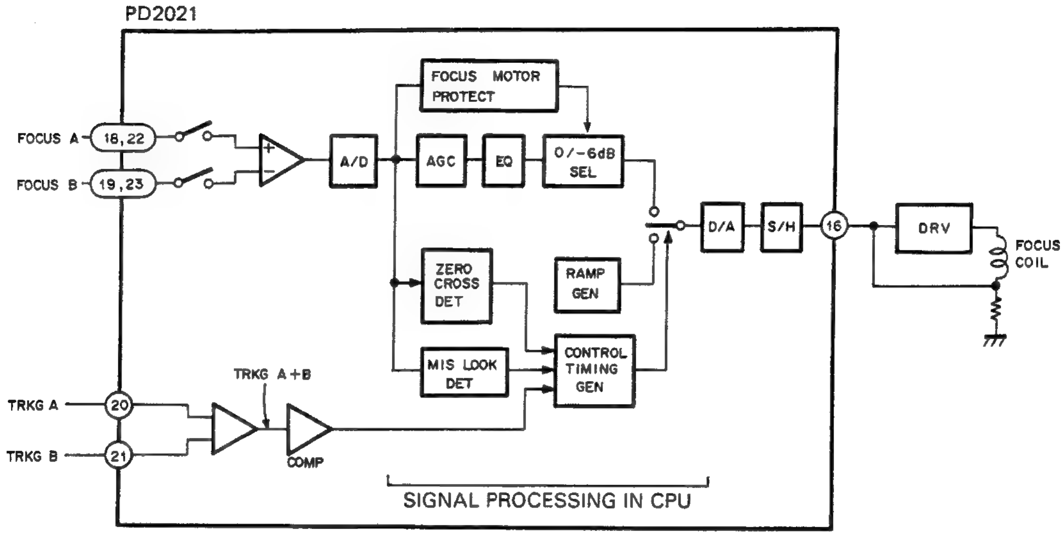


Fig. 4-2

4.3 TRACKING SERVO

The major functions of the tracking servo are as follows, and its block diagram is shown in Fig. 4-4.

1. Normal servo during play

The A/D converted tracking error data is processed by a digital filter, then output after D/A conversion.

2. Single Jump

Performs 1-track to 10-track jump operations in the still mode. The operations for 1-track jump are described below as an example. (Fig. 4-3)

① The acceleration pulse to move the lens in the jump direction is output from the Accel/Brake Pulse Generator.

② The zero-cross point of the tracking error is detected (HSZC input to pin 58 of PD2021) to output the brake pulse.

③ The on-track position is detected by the inclination of the tracking error signal to close the tracking servo.

The above series of operations starts when the JUMP TRIG signal is input to pin 54 of PD2021 after the command (with an augment indicating the number of jumps and the jump direction) is given from the main CPU.

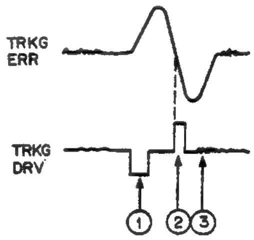


Fig. 4-3

3. Multi Jump

Performs track jumps of 10 to 100 tracks. (Same function as LD-V1000, LD-V6000A.)

During jumping, the tracking servo is opened to drive the TRKG actuator so that the relative speed between the beam and tracks is kept at a fixed level.

Detection of this relative speed is performed by measuring the period of the tracking error zero-cross signal and converting it to a frequency.

In PD2021, the detected frequency is compared with the target frequency to detect the speed error. When there are only a few tracks remaining, the tracking actuator is braked smoothly by changing the target frequency in 2 steps.

The functions of each section are as follows:
Serial-to-Parallel converter:
Converts the serial period measurement data input from PD4183 into parallel data.
Interval-to-Frequency converter:
Converts the period measurement data into frequency data by linear approximation.
Target Frequency Setting:
Sets the target frequency for frequency error detection. There are two setting methods; directly from the main CPU and by the output from the multi jump counter.
Frequency Error Detection:
Detects errors in the frequency data and the target frequency to perform the EQ operation.
This output is chiefly used to control the speed of the slider during searching. When multi jump operations are performed, it is used to control the speed of the tracking actuator.
Accel/Brake Pulse Generator (1):
Calculates the optimum value of the acceleration and braking pulses for the tracking actuator and outputs them. The frequency data and the zero-cross signal are input from the tracking zero-cross signal.
Accel/Brake Pulse Generator (2):
Calculates the acceleration and braking pulses for multi jump operations. Also switches the output between the accel/brake pulse and the frequency error detector output.

• Sections Related to Tracking Servo in PD4183 (IC5, on DSCO Board)

Track Cross Counter:
This is a 16-bit up/down counter and counts the zero-cross signal of the tracking error. The initialization and readout of the counter are performed by the main CPU via the data bus.
Track Cross Interval Counter:
This counts the period of the zero cross signal using the reference clock, when the moving direction indication (F/R) is input from the track cross decoder. The reference clock signals are the HSCAN signal (pin 7) and the TRON signal (pin 8), and they are switched over as follows:

HSCAN \ TRON	0	1
0	3.58MHz / 16	X
1	3.58MHz / 4	3.58MHz

This selection is made according to the period of the tracking zero cross signal, that is the speed with which the slider is moving .
The counted value is converted into serial data and output from pin 11 of PD4183 and input to pin 53 of PD2021.

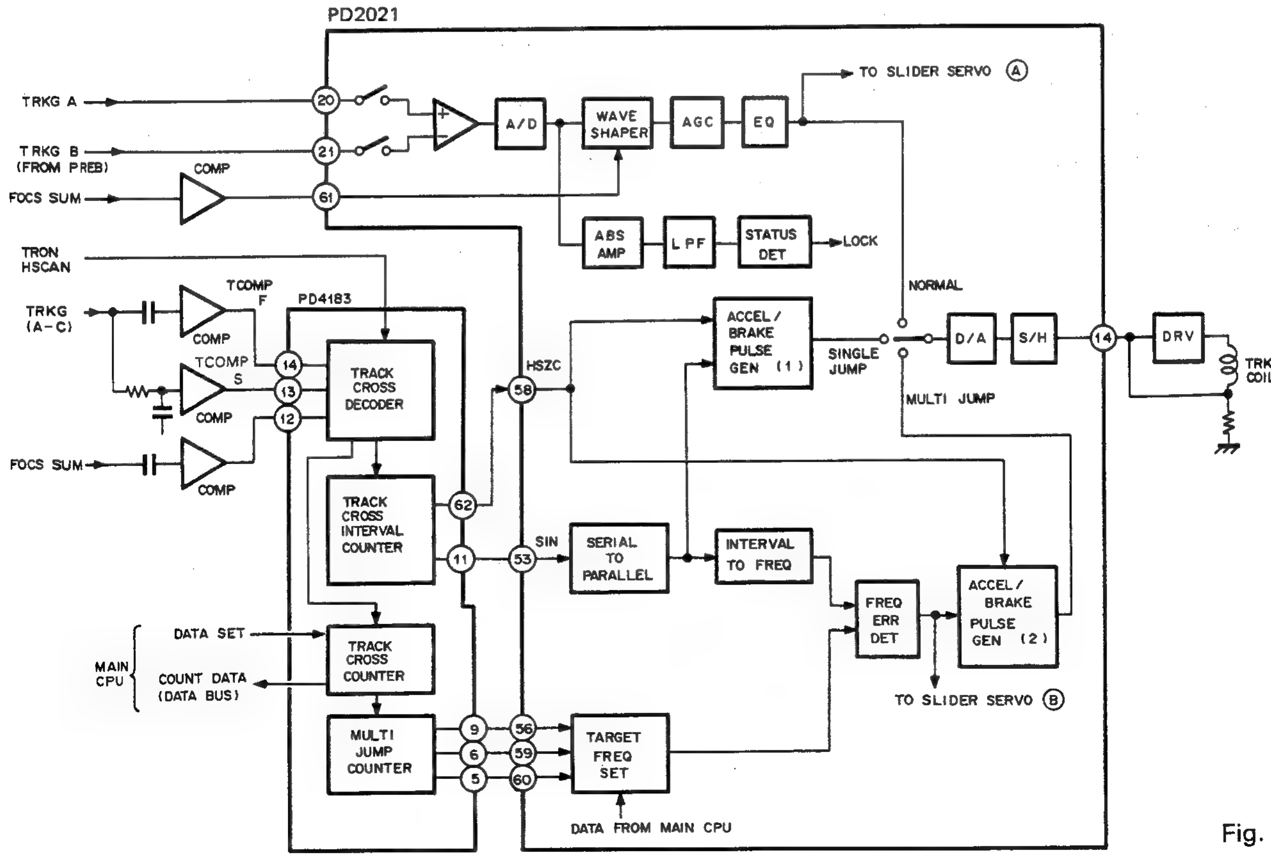


Fig. 4-4

Serial-to-parallel and period-to-frequency conversions are performed in PD2021. Speed errors are detected by comparison with the target frequency to control the tracking actuator or slider.

Track Cross Decoder:

Detects the moving direction of the slider from the phase relationship between the zero cross signal and the FCOMP signal.

Multi Jump Counter:

When multi jump operations are engaged, the count value to be jumped is set by the main CPU. Since the track cross counter is counted down, when the counting value becomes 31, 7 or 0, the MJ SLOW, MJ BRK or MJ CLR signals is output to PD2021.

4.4 SLIDER SERVO

The functions of the slider servo are described below, and its block diagram is shown in Fig. 4-5.

1. Controls the slider position from the tracking error low frequency components during play (functions when the tracking servo is closed). (Slider position error)
2. Controls the slider speed so that the tracking error frequency becomes the target value with the tracking servo open. (Slider velocity error)

The above two error signals are selected according to the operation mode and converted into the PWM signal to be output. There are two output signals from PD2021 and one of them is output as the PWM signal according to the direction in which the slider is moving.

The PWM signal is input to the PREB and flows into the drive coil.

When the slider is moved, a counterelectromotive force is generated in the speed detection coil and it passes through the Gain Control and EQ is then applied to the drive circuit as feedback.

This is to obtain the damping required by the linear motor. However, when the slider is accelerated in high-speed search, the amount of feedback is reduced by a signal from the main CPU.

Since the speed detection coil detects flux components leaking from the drive coil directly, an appropriate amount of feedback cannot be obtained without taking an appropriate countermeasure. For this, the EQ (EQ (2) in the block diagram) corresponding to the leakage flux is added to cancel it.

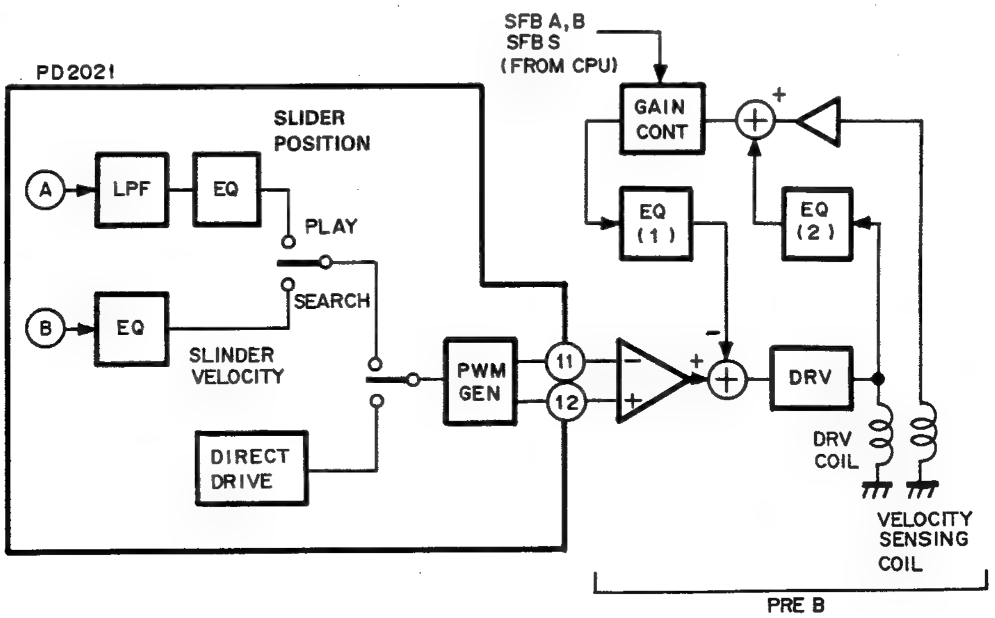


Fig. 4-5

4.5 SPINDLE SERVO

There are two servo loops in the spindle servo system.

1. FG Servo:
Detects the error in the FG signal period and the target speed (input from the main CPU) to control the spindle motor.
This is used to maintain the speed of the spindle motor when the PBH signal is not present.

2. Frequency & Phase Servo:
Detects the frequency error and the phase error from the difference in period between the PBH and SPDL REF H signals to control the spindle motor.
This servo is turned ON after the FG servo is locked; the motor is controlled by the frequency servo first, then by the phase servo when the PBH signal becomes within ± 1% of the reference level. At the same time, the digital TBC is turned ON, then the spindle servo and the TBC are working to lock the color on the screen.

The spindle servo block diagram is shown in Fig. 4-6.

In the block diagram, the section from the ERR. DET. to the point just before PWM GEN. is actually processed by the CPU in PD2021. (See the internal block diagram of PD2021.)

All the spindle servo operations are specified by commands from the main CPU, and the status data indicating the operation condition is output from PD2021. The detailed operations of the above two servo loops are as follows:

• FG Servo

The period of the FG signal (input to pin 28 of PD2021 from BLDB) is measured using the free running counter and latch. The error is detected using the difference between the measured data and the period data of the target speed. The detected error is used to perform gain adjustment and the EQ operation according to the target frequency, and is then input to the PWM generator to drive the spindle motor.
The target frequency is input as command data from the main CPU. It has a fixed value when playing CAV discs, however, it is varied according to the data from the slider position sensor when playing CLV discs. The main CPU judges whether the FG servo is locked or not using the status data from PD2021.

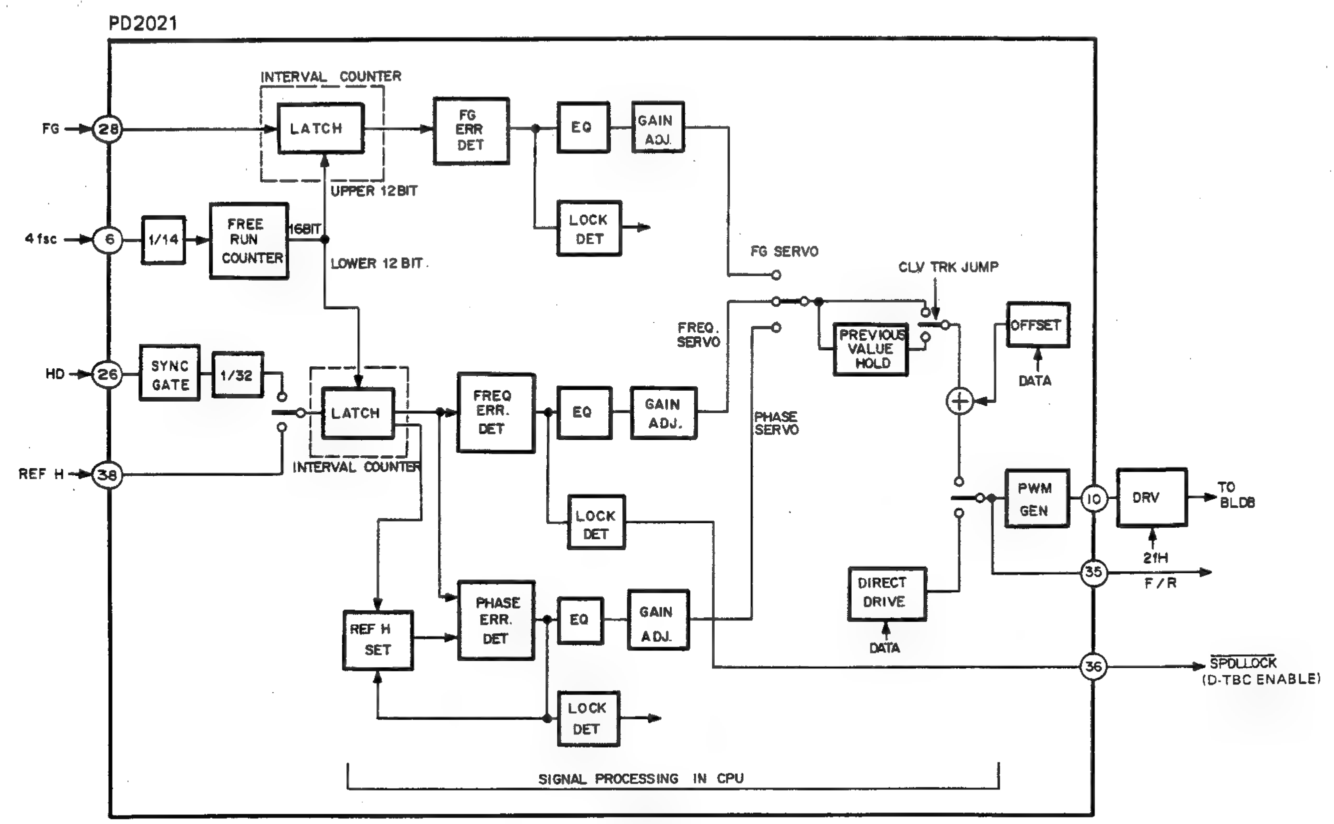


Fig. 4-6

• **Frequency & Phase Servo**

The error signal is detected as the difference between the PBH period and the SPDL REF H period using the free running counter and latch.
The clock of the free running counter is the reference 4fsc signal input to pin 6 from HD440072 on the DEGE board divided by 14. Since the SPDL REF H is obtained by dividing the 4fsc VCXO (= 910fH VCXO) which is locked to the 4fsc signal, as a result, the free running counter is division-synchronized with the SPDL REF H signal.
Since the period of the REF H signal always maintained at a fixed level, the count value can be obtained by adding the period value to the value when the edge of the previous SPDL REF H is input.
Therefore, the SPDL REF H is picked up by the CPU in PD2021 only once to match the phase with the internal reference counter from the error detection section.

The frequency servo is turned ON after the FG servo is locked, and when PBH becomes within ± 1% of the REF H period, the phase servo is turned ON. At this time, the $\overline{\text{SPDL LOCK}}$ signal at pin 36 of PD2021 goes low, and the digital TBC on the DTMC board starts operation.
When the track jump operation is engaged during the playback of CLV discs, reference shift is performed in the digital TBC section to shift the SPDL REF H signal. At this time, the RFST signal at pin 45 of PDB006 goes high to inform the main CPU that reference shift has been performed.
Then, the main CPU outputs a command to PD2021 to take in the SPDL REF H signal to perform the reference shift of the spindle servo. During jump operations, the error signal is pre-held.

• **Search Sequence: CAV long-distance search**

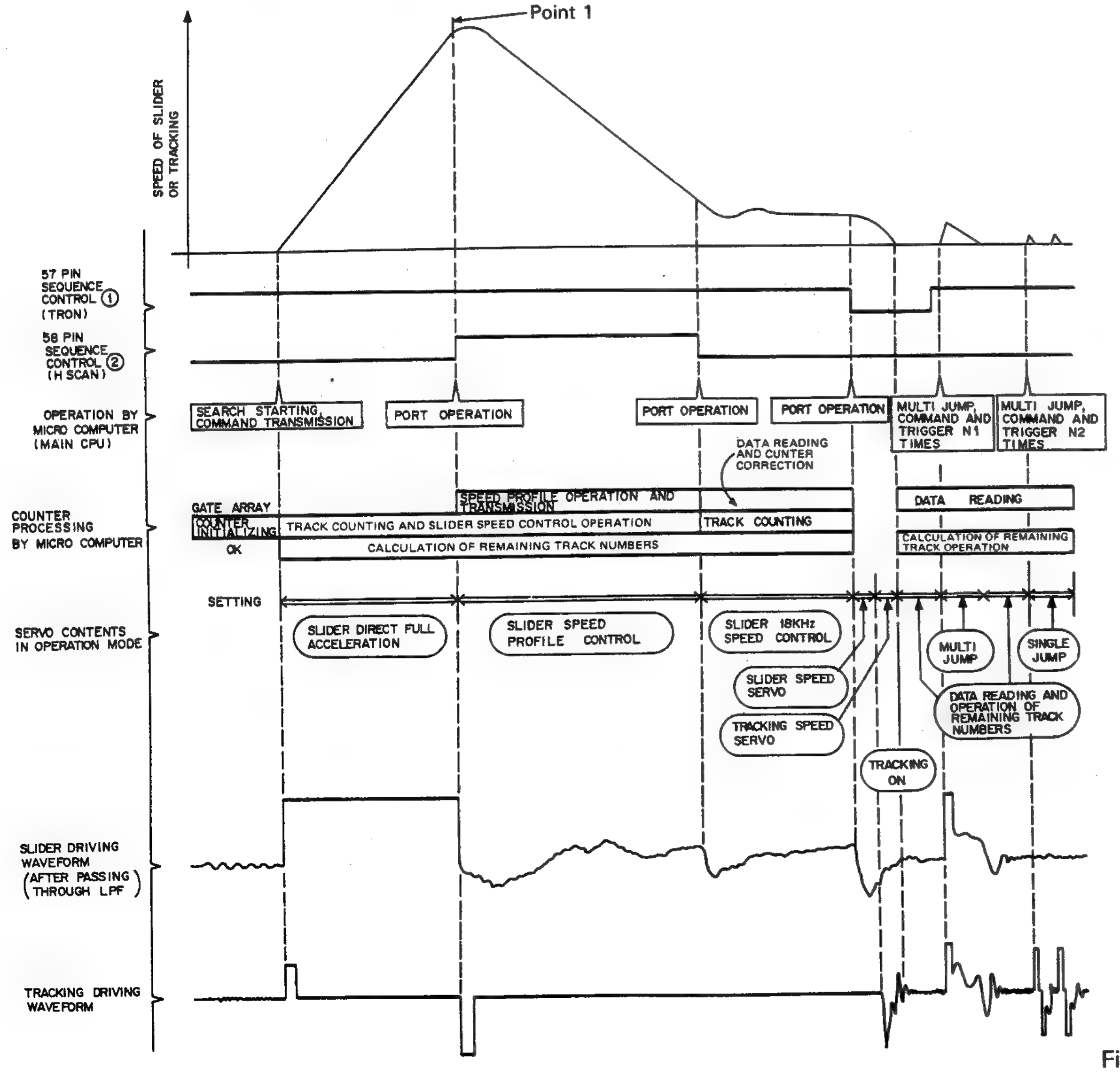
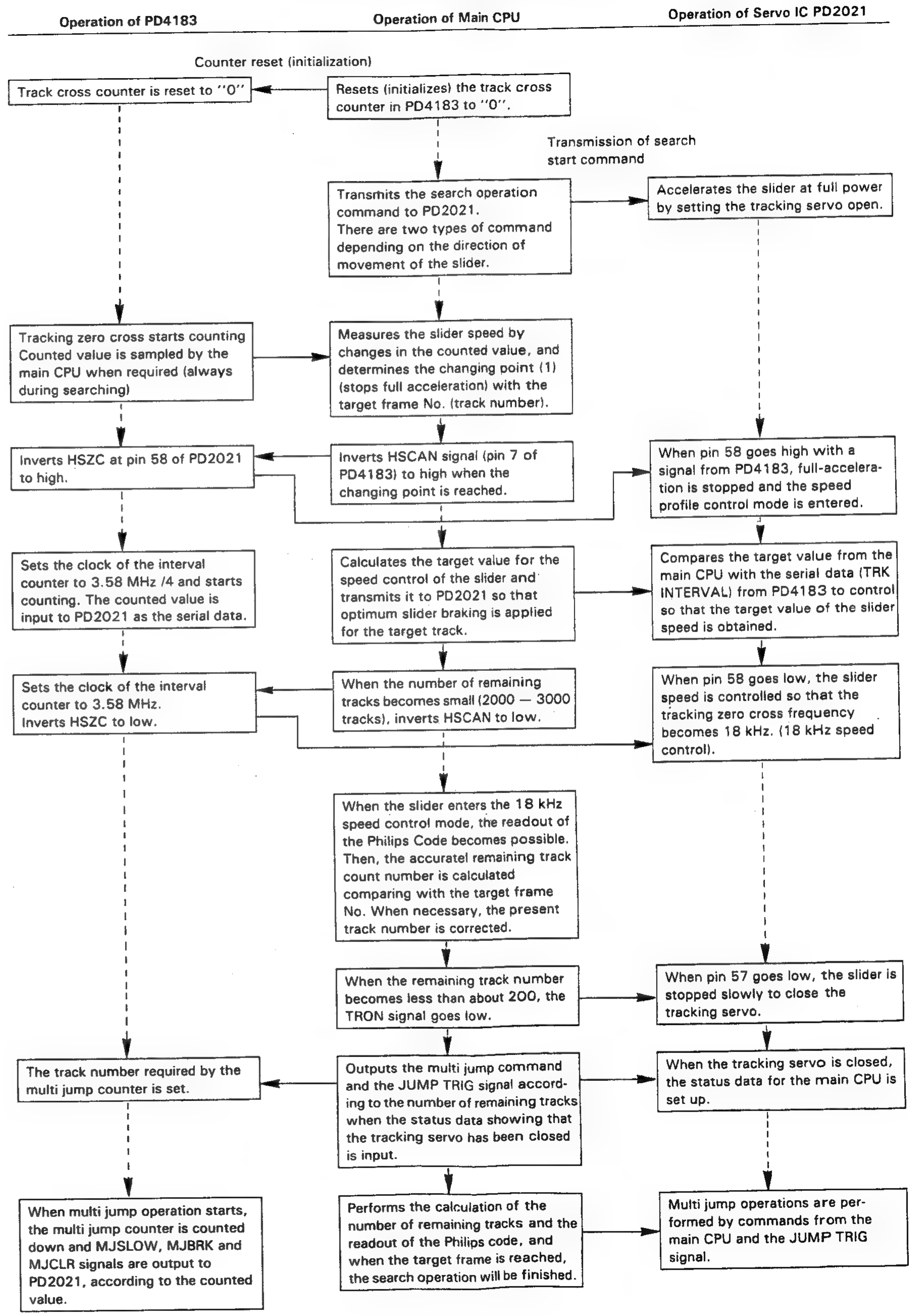
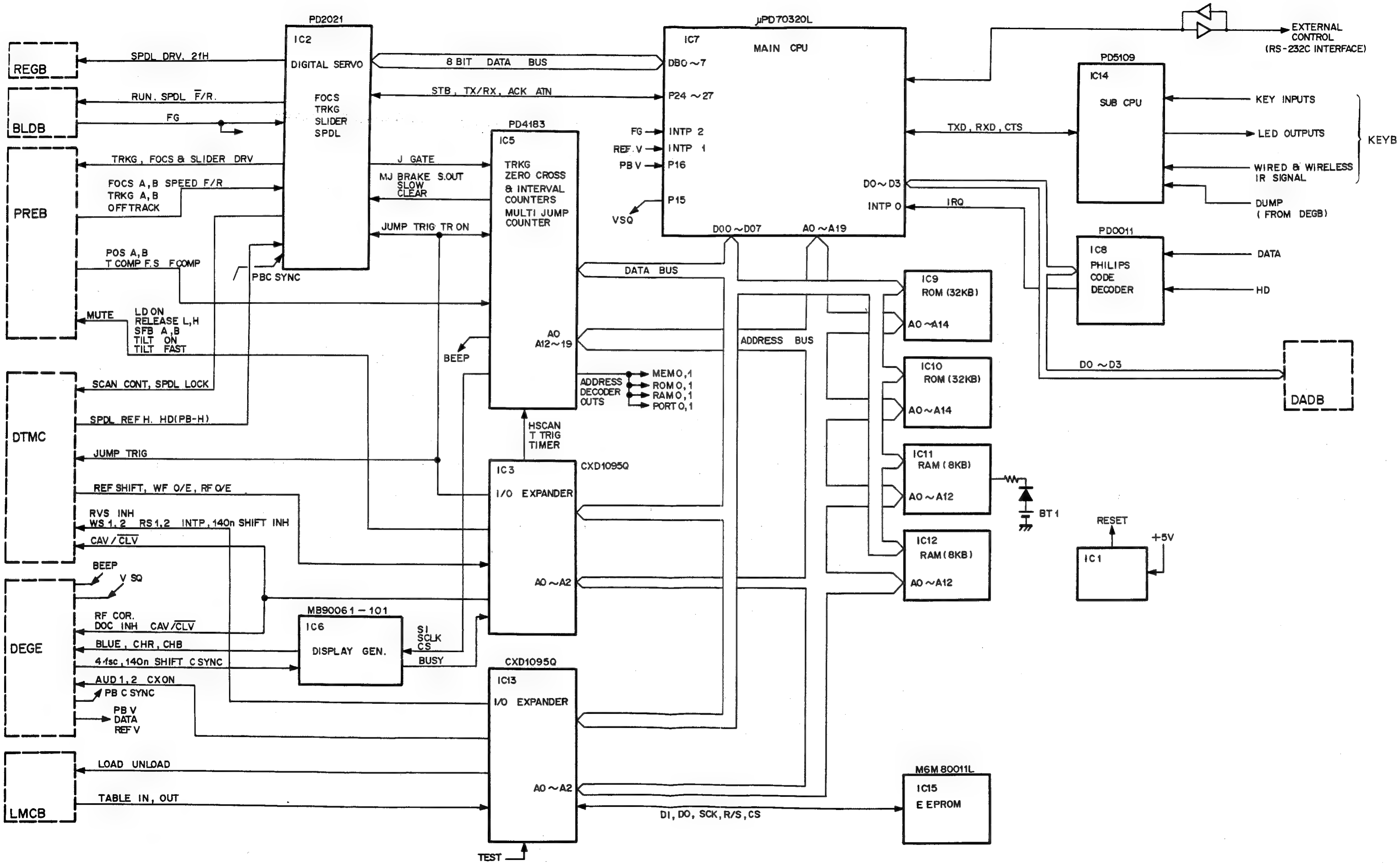


Fig. 4-7

Operation of Each Section During Searching (Description of Search Sequence)



5. CONTROL BLOCK



5.1 HARDWARE

The control block of the LD-V8000 consists of the DSCO, KEYB and JACK PC boards.

1. DSCO PC Board

The DSCO PC board contains the digital servo block as well as the control block.
The control block on the DSCO board consists of two CPUs, memory, code decoder, display, I/O ports and a gate array which includes peripheral circuits.

(1) Main CPU (IC7)
μPD70320L is used as the main CPU with a clock frequency of 9.8304 MHz. This CPU is a CMOS 16-bit 1-chip microcomputer, and has command architecture which is upward-compatible with the (Intel) 8086. As built-in peripheral devices of this CPU, a serial interface with the baud rate generator, interrupter controller, timer counter, I/O port, etc. are provided.
Two serial interfaces are provided; one is used for communications with the sub CPU. The other is connected to the interface connector on the rear panel to be used for communications with an external controller.
The PB V-SYNC (playback), REF. V-SYNC (reference) and FG signals are input to the interrupt controller. The PB V-SYNC signal is used to supply the reference timing of the player control and as the timing signal to control writing to the video memory.
The REF V-SYNC signal is used as the timing signal to control reading from the video memory.
The FG signal is used for speed detection in spindle stop processing.
There are also two timer counters; one is used as the timer for checking the time each 1 ms period. The other is the timer for backing up the V-SYNC signal. When the V-SYNC signal is not present in other than the playback mode, or when the V-SYNC signal is missing during play, the data is backed up by this timer.
The I/O ports used are ports 00 — 07, 14 — 17, 20 — 27, for a total of 20 lines. Ports 00 — 07 and 24 — 27 are used as a 8-bit parallel data bus and control signal bus. Ports 20 — 23 are used as a 4-bit parallel data bus for communications with the decoder IC and the digital audio control IC.

(2) Sub CPU (IC14)
An 8-bit CMOS 1-chip microcomputer with a clock frequency of 7.3728 MHz is used as the sub CPU. The sub CPU lights the LEDs on the main unit, reads key inputs, commands from the remote control and the dump program, etc. The LED data is transmitted from the main CPU to the RXD pin, and the read data is transmitted to the main CPU from the TXD pin as serial data. Communications of serial data are performed at 9600 bauds, with no parity, 8-bit and 1-stop bits

(3) Memory (ROM: IC9, IC10, IC15: RAM : IC11, IC12)
As the program ROM, two CMOS 32KB EPROMs (equivalent to 27C256) with a total memory capacity of 64KB, are used. As well as this, an EEP-ROM is used for saving function switch data.
As the RAM, two CMOS 8KB static RAMs (pin-compatible with 2764) with a total capacity of 16KB, are used. Since IC11 is used as the write area to dump the program, it is backed up a lithium battery. IC12 is used as the system control area for controlling the player.

(4) Code Decoder (IC8)
PD0011A is used as the code decoding IC. The code decoding IC decodes the 24-bit biphase code (Philips code) picked up from the playback video signal and inputs it into the internal RAM as data, then turns the IRQ pin low to inform the main CPU that data has been input. After the IRQ pin goes low, the main CPU reads the above data using the 4-bit parallel bus and the four control signals. The parallel bus and the control signals are also connected to the DADB board and are used to control the digital audio control CPU.

(5) Display (IC6)
MB90061-101 is used as the display IC. The display IC generates the characters and character background signals for the playback frame (time), messages, etc. according to the key input of the remote control, to be displayed on the TV screen. This is a CMOS IC having a function to generate the blue background signal which is output in the video squelch mode.
This display IC can display 128 characters as 12 lines with 20 characters per line.
The main CPU writes the characters for 2 lines in 1V period. To write characters, character data is written into the gate array by the main CPU. After the data has been written, the gate array turns the CS pin low, and converts the written data to serial data and outputs it to the SI pin, while the write clock for the display IC is output to the SCLK pin.

(6) I/O Port (IC3, IC13)
Two CXD1095Q ICs form the I/0 port. Each of the I/O port ICs has 36 ports, so a total of 72 ports are available. Some of the output and input pins of the I/O ports are connected to each other, for simple checking of the I/O ports.

(7) Gate Array (IC5)
This gate array is designed exclusively for the DSCO PC board of the LD-V8000, and includes the peripheral circuits for the control block and digital servo.

Peripheral Circuits for Control Block in IC5

1. Address Decoder
   This decodes address bus signals to generate the six chip select outputs for the ROMs, RAMs and I/O ports as well as two chip select outputs.
2. Bus Controller
   This decodes bus control signals to generate the memory read and memory write memory access signals.
3. Display IC Interface
   Converts the data written by the main CPU to synchronous serial data to be output to the display IC.
4. Beep Generator
   By writing the data into the control register, a 874 – 194 Hz frequency signal can be output. This signal is used as the source of the beep to be mixed and output as the beep signal.
5. Position Counter
   This detects the current slider position by detecting the slider moving direction with the phase difference of the signal from the position sensors (POSA, B) and sets the position counter up and down according to the direction of movement.
6. Watch Dock Timer
   This outputs the interrupt request signal from the INTRQ pin when there is no input at the TTRIG pin for a 2V period. By this, the CPU can be reset by the overrun detection signal of the CPU when an overrun occurs.
7. Remote Line Selector
   Selects either the infrared remote control input signal or the wired remote control input signal as the signal to be output to the CPU.

(8) Expansion Connector (CN100)
This is the connector for the expansion of functions.
To enable the expansion of the memory or peripheral ICs, terminal lines for the address bus, data bus, bus control signals of the main CPU are provided. It also has eight I/O ports and reset signal lines. An RS-232C and expansion connector and interface connector select switch are provided on the rear panel of the main unit.

5.2 SOFTWARE

The software of the LD-V8000 is divided into four blocks in terms of functions; a monitor block, player control block, communication control block and user block.

1 Monitor Block
Unlike the other three blocks which are used to control the player's operations, the monitor block is designed for overall control of the software.
In actual operation, it initializes the software, controls interrupts and the starting and stopping of the other three blocks, and the control of data processing/transfer between blocks, etc.

2 Player Control Block
The player control block controls the hardware of the player, and is used to perform all player operation controls including startup operations and search operations. All port control and digital servo control, etc. functions are also performed by this block.

3 Communication Control Block
The communication control block control interfacing between the player and external equipment. The major processes are as follows:

(1) Sub CPU Control
Performs LED control and command input processing, while communicating with the sub CPU using the serial interface.
LED control is performed by checking the player control block condition, and outputting the status data corresponding to the player's condition to the sub CPU as LED data.
Signals from the input keys or the remote control unit (RCU) are transmitted from the sub CPU as key data or RCU data according to the input. The data is converted into commands and stored in the command buffer.

(2) RS-232C Transmission/Reception Signal Processing
Data transmitted from an external component is stored in the receiving buffer. When the terminator signal is received, the contents of the receiving buffer are transferred to the command buffer and it waits for the next data input. In transmission, the data set in the transmission buffer is transmitted.

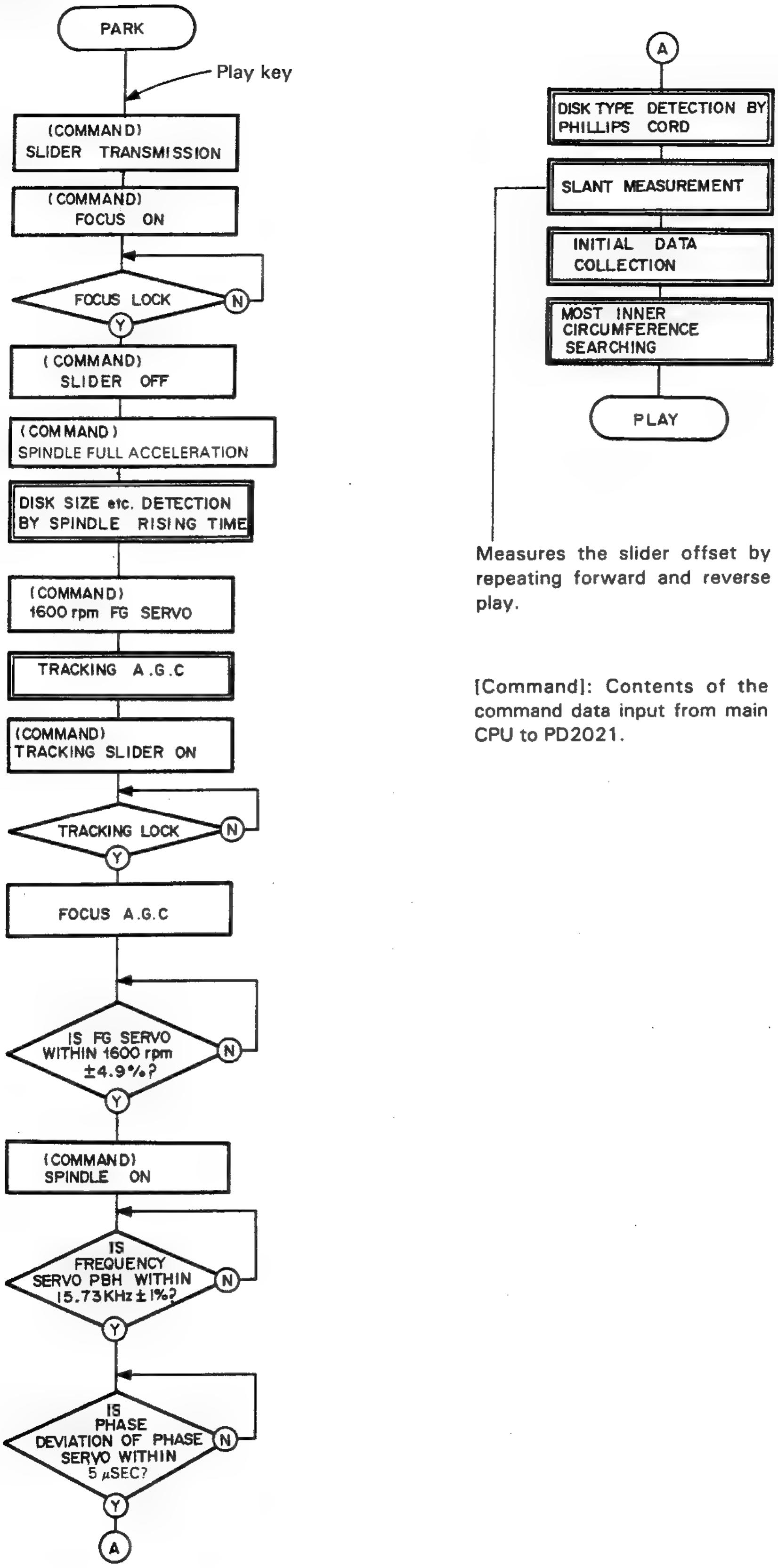
(3) Function Switch Control
This performs the readout and writing processing of the switch data from the EEP-ROM. It also performs the control of the operations set by switches.

(4) Display Control
Displays the system status including the frame/time/chapter number, audio switch setting, speed indication, etc. as well as externally input character information.

(5) Command Execution
Command execution is performed in the order from interpreting the command, transmission of the command to the player control block, execution of the transmitted command, to the monitoring of command completion.
Externally input data is stored in the command buffer as a command after each processing is performed.
Commands are interpreted by reading the command stored in the command buffer, and commands which can be processed within the communication control task will be performed as they are. If the read command could affect the player control, it is once converted to an internal command and transmitted to the player control block. When completion of the command transmitted to the player control block is to be monitored, it is checked by monitoring the status of the player control block. The above operations are repeated until the command buffer becomes empty.

4 User Block
Control of the player can be performed externally using the player control block and the communication control block. The user block is provided to enable control of the player by other than the above methods, and performs program dump processing.
In the user block, player control is performed by commands and data transmission/reception with the player control block and the communication block.

Player Startup Sequence



[Command]: Contents of the command data input from main CPU to PD2021.

6. IC INFORMATION

6.1 PD2021: IC2 (DSCO assembly)

• **Pin Functions**

Pin No.	Name (Symbol)	I/O	Function	Output Lock
1	P/S	I	Parallel/serial select for CPU interface.	
2	RESET	I	Reset input pin (Schmitt input).	
3	XROMO	I/O	(Net used)	
4	TRKFQ	O	Outputs the signal with the tracking error signal converted to logic level by the comparator. (Not used)	FGIN
5	XOUT	O	External clock output pin.	
6	XIN	I	External clock input pin. 4fsc input.	
7	REFSC	O	Outputs the signal with the clock frequency input to XIN pin divided by four.	C-SYNC
8	REF2H	O	Outputs the signal with the clock frequency input to XIN pin divided by 455.	C-SYNC
9	REFH	O	Outputs the reference H signal for the internal sync generator. (Not used)	C-SYNC
10	SPDLDRV	O	Spindle PWM output pin.	SIN
11	SLDDRV +	O	Slider PWM output pin.	SIN
12	SLDDRV −	O	Slider PWM output pin.	SIN
13	—	O	Open	
14	TRKOUT	O	Tracking drive output.	
15	VM	O	1/2 V reference output.	
16	FCSOUT	O	Focus drive output.	
17	Vss-A	—	GND for analog circuits.	
18	FCSA	I	Focus A input.	
19	FCSB	I	Focus B input.	
20	TRKA	I	TRKG (Tracking) A input.	
21	TRKB	I	TRKG B input.	
22	FCSA	I	Focus A input.	
23	FCSB	I	Focus B input.	
24	VREF	I	V reference input.	
25	Vdd-A	—	Power supply for analog circuits.	
26	CSYNC	I	PB C-Sync input.	
27	DOCINH	O	DOC INH signal output (Not used).	C-SYNC
28	FGIN	I	FG input pin.	
29	RREFF	I	Reference frame input pin. Pulled-up	
30	TESTO	I	Connect the Vdd-A (25 pin).	
31	TEST1	I	Pulled-up	
32	TEST2	I	Connect the Vdd-A (25 pin).	
33	Vss-D	—	GND for digital circuits.	
34	SCAN CONT	O	SCAN control signal output.	
35	SPDL $\overline{F}$/R	O	SPDL F/R signal output.	
36	$\overline{\text{SPDLLOCK}}$	O	SPDL lock signal output.	
37	J GATE	O	Jump gate output.	
38	PB4	I	SPDL (Spindle) reference H input.	
39	Vdd-D	—	Power supply for digital circuits.	
40	$\overline{\text{ATN}}$	I	Inputs the timing signal for transmitting the device-exclusive address to the CPU interface.	
41	$\overline{\text{ACK}}$	O	Outputs the signal which indicates the busy/ready status for data transmission with CPU. Open drain output.	STB

Pin No.	Name (Symbol)	I/O	Function	Output Lock
42	TX/$\overline{\text{RX}}$	I	Sets the data transmission direction for CPU interface.	
43	$\overline{\text{STB}}$	I	Inputs the data transmission timing signal of CPU interface. Inputs the shift clock in the serial operation mode.	
44	DB0	I/O	LSB data I/O pin when CPU interface operates in parallel. Serial output pin in the serial mode.	
45	DB1	I/O	2nd LSB data I/O pin when CPU interface operates in parallel. Serial output pin in the serial mode.	
46	DB2	I/O		
47	DB3	I/O		
48	DB4	I/O	Parallel data I/O pin when the CPU interface operates in parallel.	
49	PB5	I/O		
50	DB6	I/O		
51	DB7	I/O		
52	SOUT	O	Output pin for high-speed serialoutput. (Not used)	SIN
53	SIN	I	Input pin for high-speed serial input.	
54	JUMPTRIG	I/O	Jump TRIG (trigger) input.	
55	SPEED	I/O	Speed F/R input.	
56	MJ SLOW	I/O	Multi-jump slow input.	
57	TR ON	I/O	Tracking ON input.	
58	HSZC	I/O	High-Scan or zero-cross input.	
59	MJ BRAKE	I/O	Multi-jump brake input.	
60	MJ CLEAR	I/O	Multi-jump clear input.	
61	OFF TRACK	I/O	Off-track input.	
62	XROM3	I/O	(Not used)	
63	XROM2	I/O	(Not used)	
64	XROM1	I/O	(Not used)	

6.2 PD4183 (Gate Array): IC5 (DSCO assembly)

• Pin Functions

Pin No.	Name	I/O	Function
1	POSB	I	Position sensor B-phase input.
2	POSA	I	Position sensor A-phase input.
3	2FH	I	2-times H input (31.5 kHz).
4	FSC	I	Sub-carrier input (3.579545 MHz).
5	MJCLR	O	Outputs high level signal when the LSB of the jump counter is "0".
6	MJBRK	O	Outputs high level signal when the LSB of the jump counter is "7".
7	HSCAN	I	High-Scan ON at high level.
8	$\overline{\text{TRON}}$	I	Tracking ON at low level.
9	HJSLOW	O	Outputs high level signal when the LSB of the jump counter is "31".
10	$\overline{\text{JPTRIG}}$	I	Jump counter starts counting at high level.
11	$\overline{\text{SOUT}}$	O	Serial output of zero-cross interval counter.
12	$\overline{\text{JGATE}}$	I	Holds the interval counter at low level.
13	TCOMPS	I	Tracking zero-cross input (after LPF for LDD).
14	TCOMPF	I	Tracking zero-cross input.
15	FCOMP	I	Focus zero-cross input.
16	FGIN	I	GND
17	FGOUT	O	NC (No connection)

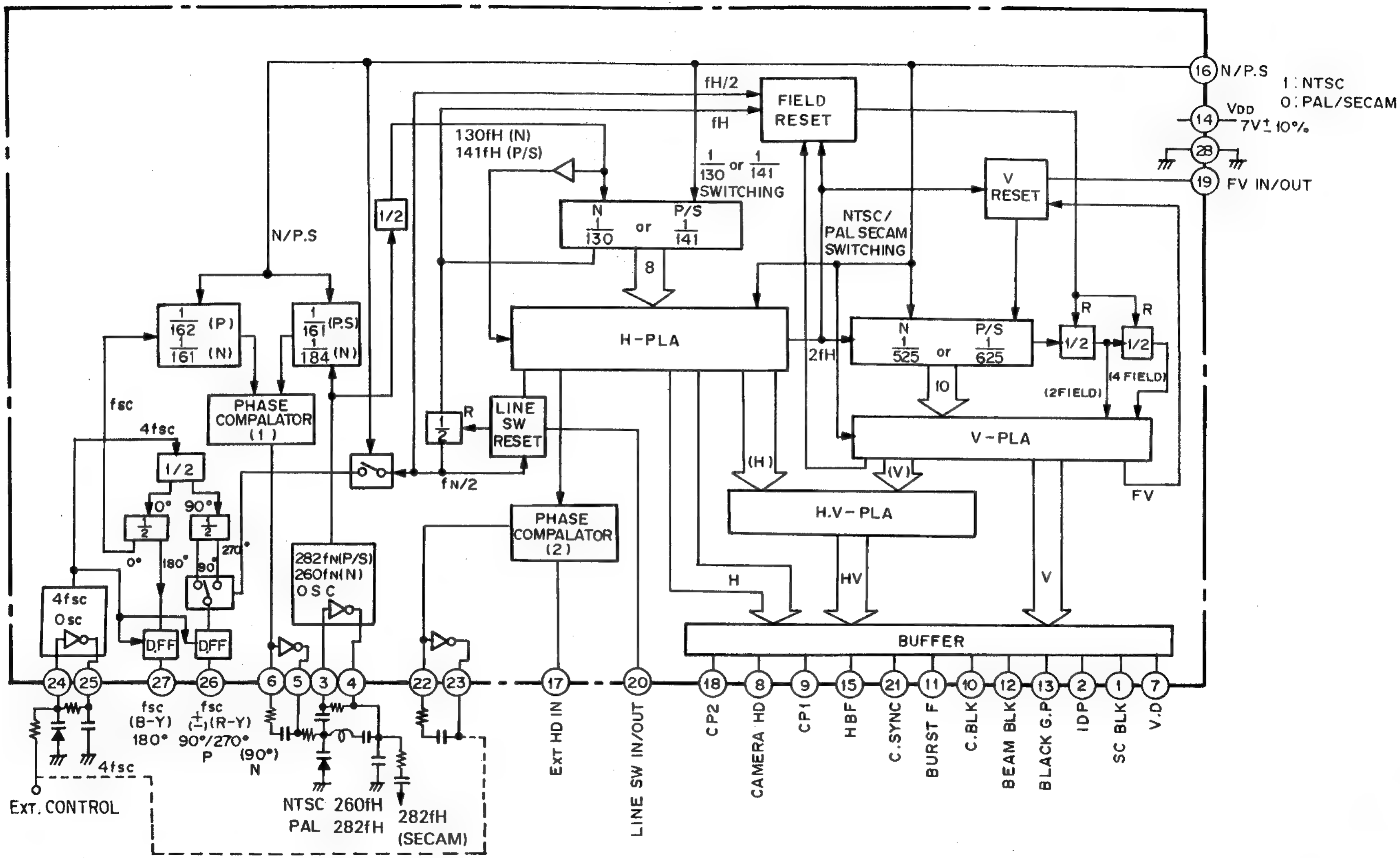
Pin No.	Name	I/O	Function
18	SCLK	O	Clock output for serial communication with display IC.
19	SI	O	Data output for serial communication with display IC.
20	$\overline{\text{DISPLAY}}$	O	Select output for serial communication with display IC.
21	$\overline{\text{MEMRD}}$	O	Outputs the low level signal for output request to the external device.
22	$\overline{\text{MEMWR}}$	O	Outputs the low level signal for input request to the external device.
23	GND	–	
24	$\overline{\text{MEM0}}$	O	Outputs the low level signal when selecting the extension memory "0".
25	$\overline{\text{MEM1}}$	O	Outputs the low level signal when selecting the extension memory "1".
26	$\overline{\text{ROM0}}$	O	Outputs the low level signal when selecting the external ROM "0".
27	$\overline{\text{ROM1}}$	O	Outputs the low level signal when selecting the external ROM "1".
28	$\overline{\text{RAM0}}$	O	Outputs the low level signal when selecting the external RAM "0".
29	$\overline{\text{RAM1}}$	O	Outputs the low level signal when selecting the external RAM "1".
30	$\overline{\text{PORT0}}$	O	Outputs the low level signal when selecting the extension port "0".
31	$\overline{\text{PORT1}}$	O	Outputs the low level signal when selecting the extension port "1".
32	Vss	–	
33	A19	I	Address bus A19
34	A18	I	Address bus A18
35	A17	I	Address bus A17
36	A16	I	Address bus A16
37	A15	I	Address bus A15
38	A14	I	Address bus A14
39	A13	I	Address bus A13
40	A12	I	Address bus A12
41	A00	I	Address bus A00
42	D07	I/O	Data bus D07
43	D06	I/O	Data bus D06
44	D05	I/O	Data bus D05
45	D04	I/O	Data bus D04
46	GND	–	
47	D03	I/O	Data bus D03
48	D02	I/O	Data bus D02
49	D01	I/O	Data bus D01
50	D00	I/O	Data bus D00
51	$\overline{\text{MREQ}}$	I	Accesses the bus at low level.
52	R/$\overline{\text{W}}$	I	Read (high)/write (low) input
53	$\overline{\text{INTRQ}}$	O	Outputs low level signal when watchdog timer overflows.
54	REFV	I	Clock input (60 Hz) for watchdog timer.
55	$\overline{\text{TIMER}}$	I	Permits operation of watchdog timer at low level.
56	$\overline{\text{TTRIG}}$	I	Resets the watchdog timer at low level.
57	$\overline{\text{IR}}$	I	Remote control signal input from RCU.
58	SELECT	I	RCU (low)/WIRE (high) select signal input.
59	WIRE	I	Inputs the signal from wired remote control, etc.
60	$\overline{\text{REM}}$	O	RCU/WIRE select output.
61	BEEP	O	Beep source output.
62	HSZC	O	High-Scan/zero-cross select output.
63	$\overline{\text{RESET}}$	I	Reset input.
64	Vdd	–	

6.3 HD440072 (Sync Signal Generator): IC4 (DEGE assembly)

• **Pin Functions**

Pin No.	Name	Function
1	SC.BLK	SECAM identification pulse. (Not used)
2	ID.P	SECAM identification pulse. (Not used)
3	$260f_H/282f_H$ osc	260 fH VCO input.
4	$260f_H/282f_H$ osc	260 fH VCO output.
5	Filter	out
6	Filter	in
7	VD	Reference V output.
8	Camera HD	Not used.
9	C.P1	Not used.
10	Composite BLK	Not used.
11	Bust Flag P	Not used.
12	Beam BLK	Not used.
13	Black Gate P	Not used.
14	V_{DD}	Power supply pin.
15	HBF	Not used.
16	Selector input	At high level in NTSC mode. At low level in PAL, SECAM modes. (NTSC/PAL SECAM)
17	Ext. HDin	H Genlock input pin. (External HD input for H Genlock.)
18	C.P2	Not used.
19	FV in/out	External V sync signal input/output
20	Line SW in/out	Not used.
21	Composite Sync	Composite sync output.
22	Filter	in
23	Filter	out
24	$4f_{SC}$ osc	4fsc VCXO input.
25	$4f_{SC}$ osc	4fsc VCXO output.
26	SC (90°/270°)	Only 90° (pin 16 is at high level) in the NTSC mode. (Not used)
27	SC (180°)	Reference sub-carrier output.
28	GND	GND

- **Block Diagram**

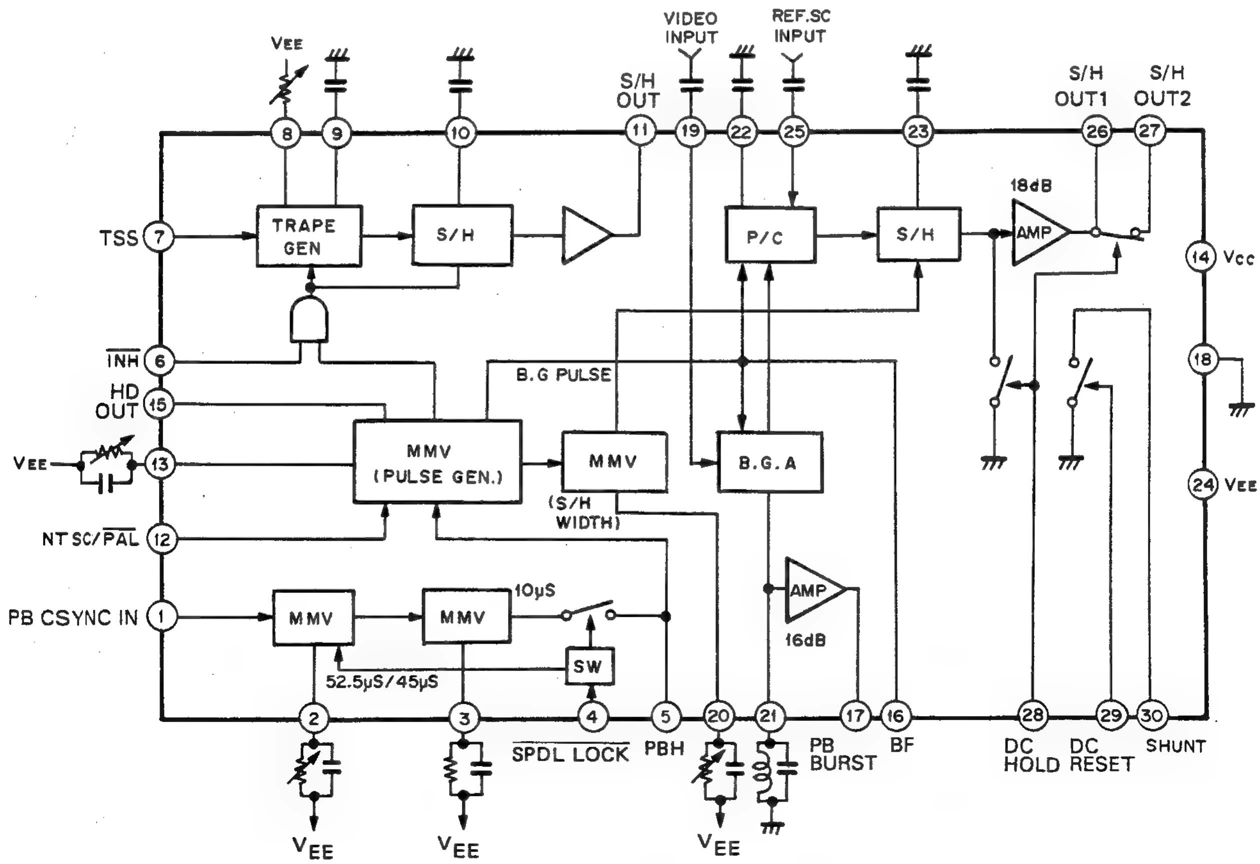


6.4 PA5012: IC1 (DTMC assembly)

• Pin Functions

Pin No.	Name	Function	Pin No.	Name	Function
1	PB CSYNC	PB C-sync input.	16	BF	Burst flag output.
2	—	Time constant for MMV.	17	PB Burst	PB burst output.
3	—	Time constant for MMV.	18	GND	
4	$\overline{\text{SPDLLOCK}}$	SPDL (Spindle) lock input.	19	PB VIDEO	PB video input.
5	PBH	PB H-sync output.	20	—	Time constant for MMV.
6	$\overline{\text{INH}}$	S/H inhibit input.	21	—	Time constant for burst gate amp.
7	TSS	Reference H input	22	—	Capacitor for phase comparator.
8	—	Resistor for TRAPE generator.	23	—	Capacitor for S/H block.
9	—	Capacitor for TRAPE generator.	24	VEE	
10	—	Capacitor for S/H block	25	REFSUB	Reference sub-carrier input.
11	S/H OUT	H-error output.	26	S/H OUT1	VPS error output.
12	NTSC/$\overline{\text{PAL}}$	NTSC/$\overline{\text{PAL}}$ select input	27	S/H OUT2	Switched error output.
13	—	Time constant for MMV.	28	DC HOLD	DC hold input.
14	Vcc	Power supply pin	29	DC RESET	DC reset input.
15	HDOUT	Horizontal drive output.	30	SHUNT	

• Block Diagram



- **6.5 PDB005: IC3 (DTMC assembly)**
- **Pin Functions**

Pin No.	I/O	Name	Function
1	I	56NIN	560N window input.
2	O	56NOUT	560N window output.
3	O	PCR	Playback (PB) chroma judgment signal output.
4	O	WF	Playback (PB) field judgment signal output. Odd: High.
5	O	WV	Playback (PB) vertical sync signal output.
6	I	NTBH	Active high when line memory is in the 1H fixed mode.
7	I	CKH	Write counter hold signal input. Hold: High.
8	I	NSPLOC	SPDL (Spindle) lock input. Lock: Low.
9	I	PH	Playback (PB) horizontal sync signal input.
10	I	CKIN	Write clock input.
11	O	QOUT	D-latch output. (Open)
12	I	LAT	D-latch clock input. (GND)
13	I	DIN	D-latch data input. (GND)
14	I	SEL	Test input. (GND)
15	I	TESTIN	Test input. (GND)
16	I	DCTIN	Write position detect time constant input.
17	O	DCTOUT	Write position detect time constant output.
18	O	NOUT	NAND output. (Open)
19	I	NIN2	NAND input 2. (GND)
20	I	NIN1	NAND input 1. (GND)
21	O	TREFH	T.S.S. output (TRAPE starts at the sinking edge).
22	O	SHINH	Inhibits the H-error sampling. Inhibit: Low
23	I	RESET	Test input.
24	–	VSS	GND
25	–	VDD	+5 V power supply.
26	O	DCREST	Burst DC error reset. Reset: high
27	O	RESC	REF SC (Reference sub-carrier) output.
28	O	DLYOUT	REF SC (time constant) output.
29	I	DLYIN	REF SC (time constant) input.
30	O	REFMON	REF SC monitor output. (Open)
31	I	BF	Burst flag input.
32	I	FBIN	Playback (PB) burst input.
33	O	FBOUT	Playback (PB) burst amp output.
34	I	DOSE	Dropout signal input. Dropout: High
35	I	PV	Playback (PB) vertical sync signal input.
36	–	VDD	+5 V power supply.
37	–	VSS	GND
38	O	NCK	Write clock invert output.
39	O	CK	Write clock output.
40	I	D17	Video data input (MSB) from the A/D converter.
41	I	D16	Video data input from the A/D converter.
42	I	D15	Video data input from the A/D converter.
43	I	D14	Video data input from the A/D converter.
44	I	D13	Video data input from the A/D converter.
45	I	D12	Video data input from the A/D converter.

Pin No.	I/O	Name	Function
46	I	D11	Video data input from the A/D converter.
47	I	D10	Video data input (LSB) from the A/D converter.
48	I	CRTIN	Chroma judgment time constant input.
49	O	CRTOUT	Chroma judgment time constant output.
50	I	RDCK	Read clock input.
51	I	FRSTR	Line memory read reset input.
52	O	D00	Video data output (LSB) to the line memory.
53	O	D01	Video data output to the line memory.
54	O	D02	Video data output to the line memory.
55	O	D03	Video data output to the line memory.
56	–	VDD	+5 V power supply.
57	–	VSS	GND
58	–	–	N.C
59	O	FRSTW	Line memory write reset output.
60	O	FCK	Write clock output to the line memory.
61	O	D04	Video data output to the line memory.
62	O	D05	Video data output to the line memory.
63	O	D06	Video data output to the line memory.
64	O	D07	Video data output (MSB) to the line memory.

6.6 PDB006: IC14 (DTMC assembly)

- **Pin Functions**

Pin No.	I/O	Name	Function
1	–	–	NC
2	–	VSS	GND
3	O	A7	R/W (Read/Write) V-address time-division output.
4	O	A6	R/W (Read/Write) H-address time-division output.
5	O	A5	R/W (Read/Write) H-address time-division output.
6	O	A4	R/W (Read/Write) H-address time-division output.
7	O	A3	R/W (Read/Write) H-address time-division output.
8	O	A2	R/W (Read/Write) H-address time-division output.
9	O	A1	R/W (Read/Write) H-address time-division output.
10	O	A0	R/W (Read/Write) H-address time-division output.
11	O	NCE	Field memory chip enable. ($\overline{CE}$)
12	O	MNWE2	Field memory 2 write enable (at LSB side).
13	O	MNWE1	Field memory 1 write enable (at MSB side).
14	O	NWSRS	Field memory R/W strobe.
15	O	TMD7	Video data (MSB) to be written to the field memory.
16	O	TMD6	Video data to be written to the field memory.
17	O	TMD5	Video data to be written to the field memory.
18	–	VDD	+5 V power supply.
19	O	TMD4	Video data to be written to the field memory.
20	–	VSS	GND
21	O	RDCK1	4Fsc output.
22	I	FMD7	Video data (MSB) read from the field memory.
23	I	FMD6	Video data read from the field memory.
24	I	FMD5	Video data read from the field memory.
25	I	FMD4	Video data read from the field memory.
26	O	TMD3	Video data to be written to the field memory.
27	O	TMD2	Video data to be written to the field memory.
28	O	TMD1	Video data to be written to the field memory.
29	O	TMD0	Video data (LSB) to be written to the field memory.
30	I	FMD3	Video data read from the field memory.
31	I	FMD2	Video data read from the field memory.
32	I	FMD1	Video data read from the field memory.
33	I	FMD0	Video data (LSB) read from the field memory.
34	O	SPREF	Spindle reference output.
35	I	SFTIH	Reference shift inhibit input. Inhibit: High
36	I	CRO	Spindle lock detect time constant input.
37	–	–	NC (no connection).
38	–	–	NC (no connection).
39	–	VSS	GND
40	O	CR1	Spindle lock detect time constant output.
41	O	TMON3	Test output (SGEH: S.G. H/2REJ output)
42	O	WVCLK	Write V-address clock output.
43	O	DCHOLOD	Burst DC error hold. Hold: High
44	I	PH	Playback horizontal sync signal input. (Playback H)
45	O	NSPLOC	Spindle lock output. ($\overline{SPDL\ LOCK}$) Lock: Low

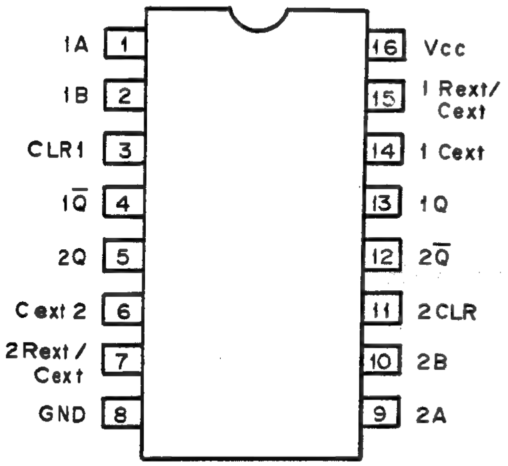
Pin No.	I/O	Name	Function	
46	O	CKH	Write counter hold signal output.	Hold: High
47	O	NTBH	At high level when the line memory is in the 1H fixed mode.	
48	I	WV	Playback vertical sync signal input (from PDB005).	
49	I	WF	Playback field judgment signal input (Write flag).	Odd: High
50	I	PCR	Playback chroma judgment signal input. (Playback chroma)	
51	O	TFD7	Video data output to the line memory (1H fixed mode).	
52	O	TFD6	Video data output to the line memory (1H fixed mode).	
53	O	TFD5	Video data output to the line memory (1H fixed mode).	
54	O	TFD4	Video data output to the line memory (1H fixed mode).	
55	–	VSS	GND	
56	I	ART	Write area control input.	Write enable: High
57	–	VDD	+5 V power supply.	
58	I	FFD7	Video data output (MSB) to the line memory.	
59	I	FFD6	Video data output to the line memory.	
60	I	FFD5	Video data output to the line memory.	
61	I	FFD4	Video data output to the line memory.	
62	O	RDCK2	4Fsc output. (read clock 2)	
63	O	FRSTR	Line memory read reset.	
64	O	NRE	Line memory read enable. ($\overline{RE}$)	Enable: Low
65	I	FFD3	Video data output to the line memory.	
66	I	FFD2	Video data output to the line memory.	
67	I	FFD1	Video data output to the line memory.	
68	I	FFD0	Video data (LSB) output to the line memory.	
69	O	TFD3	Video data output to the line memory (1H fixed mode).	
70	O	TFD2	Video data output to the line memory (1H fixed mode).	
71	O	TFD1	Video data output to the line memory (1H fixed mode).	
72	O	TFD0	Video data output to the line memory (1H fixed mode).	
73	–	VDD	+5 V power supply.	
74	–	–	NC (No connection)	
75	–	–	NC (No connection)	
76	–	VSS	GND	
77	I/O	ODCR	DC hold signal detect time constant input/output	
78	O	TMON1	Test output [WV2: Write V-address 2 output].	
79	O	TMON2	Test output [RV2: Read V-address 2 output].	
80	I	ACBR	Acceleration/deceleration signal input. (GND)	Acceleration: High
81	O	SPERR	PWM spindle error output. (Open)	
82	O	DFH	Fsc/128 output.	
83	O	OD7	Video data output (MSB).	
84	O	OD6	Video data output.	
85	O	OD5	Video data output.	
86	O	OD4	Video data output.	
87	O	OD3	Video data output.	
88	O	OD2	Video data output.	
89	O	OD1	Video data output.	
90	O	OD0	Video data output (LSB).	

Pin No.	I/O	Name	Function
91	O	RDCK3	4Fsc output.
92	–	VSS	GND
93	I	CKINV	RDCK3 output select control input. (Clock invert) Invert: High
94	–	VDD	+5 V power supply.
95	O	HBL	Horizontal blanking output.
96	I	HBLRTN	Horizontal blanking return input.
97	O	HBLS	140n shift horizontal blanking output.
98	O	RV	Read field timing output.
99	I	SGEC	Reference C-sync input.
100	O	CSYNC	140n shift S.G C-sync output. (Open)
101	O	CBL	H-V sync insert control output. (Composite blanking)
102	O	CRMINV	140n shift control output. (Chroma invert)
103	I	N14SHI	Digital 140n shift control input. 2CKDLY: High
104	O	SGCSOT	S.G C-sync output.
105	I	SGCSIN	140n DLY S.G C-sync input.
106	I	CLR1	Test input.
107	I	CLR2	Test input.
108	I	HIZ	Test input.
109	I/O	DLCR	Read position adjustment time constant input/output.
110	I	CKIN	VCXO oscillator input.
111	–	–	NC (No connection)
112	–	–	NC (No connection)
113	O	CKOUT	VCXO oscillator output.
114	O	PDO	VCXO error output. (Phase detector output)
115	I	MD1	Test input.
116	I	MD2	Test input.
117	I	MD3	Test input.
118	I	NRVSIH	Address shift inhibit input. Inhibit: High
119	O	R358	Read 3.58 MHz output.
120	O	RCRM	Read chroma judgment signal output. (Read chroma)
121	O	WFMON	Write field judgment signal output (Write field monitor). Odd: High
122	O	RFMON	Read field judgment signal output (Read field monitor). Odd: High
123	I	JP	Jump trigger input.
124	I	SCNCNT	Scan control input.
125	I	NCLV	CAV/$\overline{\text{CLV}}$ (input). CLV: Low
126	I	WRE1	Field memory 1 write control input. Write enable: High
127	I	WRE2	Field memory 2 write control input. Write enable: High
128	I	A	Multi/Bit parameter input
129	–	VDD	+5 V power supply.
130	I	SFINH	Art/Multi inhibit input. Inhibit: High
131	–	VSS	GND
132	I	B	Multi/Bit parameter input.
133	I	MLTON	Multi control input. Multi mode: High
134	I	ARTON	ART control input. Art mode: High
135	I	TWON	2-screen control input. 2-screen mode: High

Pin No.	I/O	Name	Function	
136	I	ZNZON	After-image control input.	After-image mode: High
137	I	SOLON	Solarization control input.	BIT mode: High
138	I	INTP	Interpolation control input.	Interpolation mode: High
139	I	NSTB	Trick playback control signal strobe input. ⊔	
140	O	A14	R/W V-address time-division output.	
141	O	A13	R/W V-address time-division output.	
142	O	A12	R/W V-address time-division output.	
143	O	A11	R/W V-address time-division output.	
144	O	A10	R/W V-address time-division output.	
145	O	A9	R/W V-address time-division output.	
146	O	A8	R/W V-address time-division output.	
147	—	VDD	+5 V power supply.	
148	—	—	NC (No connection)	

6.7 HD74HC221

- **Pin Functions**



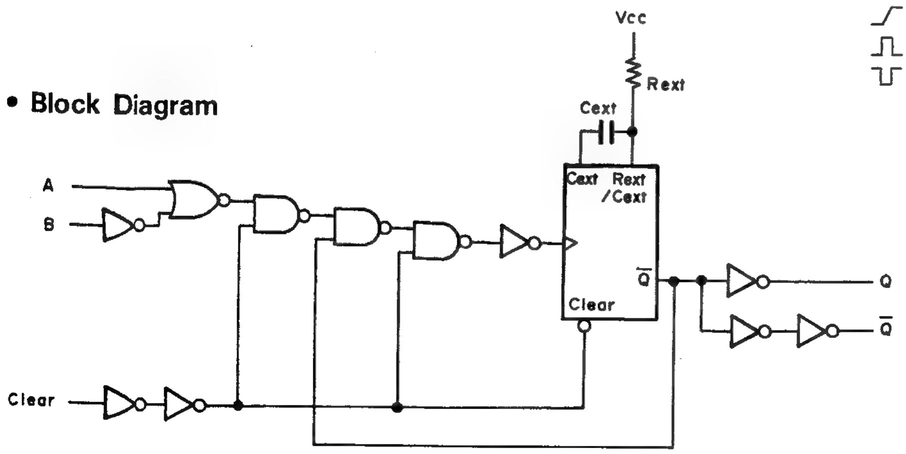
(Top View)

- **Function Table**

Input			Output	
Clear	A	B	Q	Q̄
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	╱	⎍	⊔
H	╲	H	⎍	⊔
╱	L	H	⎍	⊔

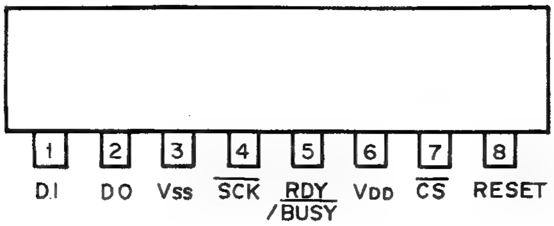
H: High level
L: Low level
X: Don't care (either high or low).
╲: Inversion from high to low.
╱: Inversion from low to high.
⎍: Single high-level pulse.
⊔: Single low-level pulse.

- **Block Diagram**

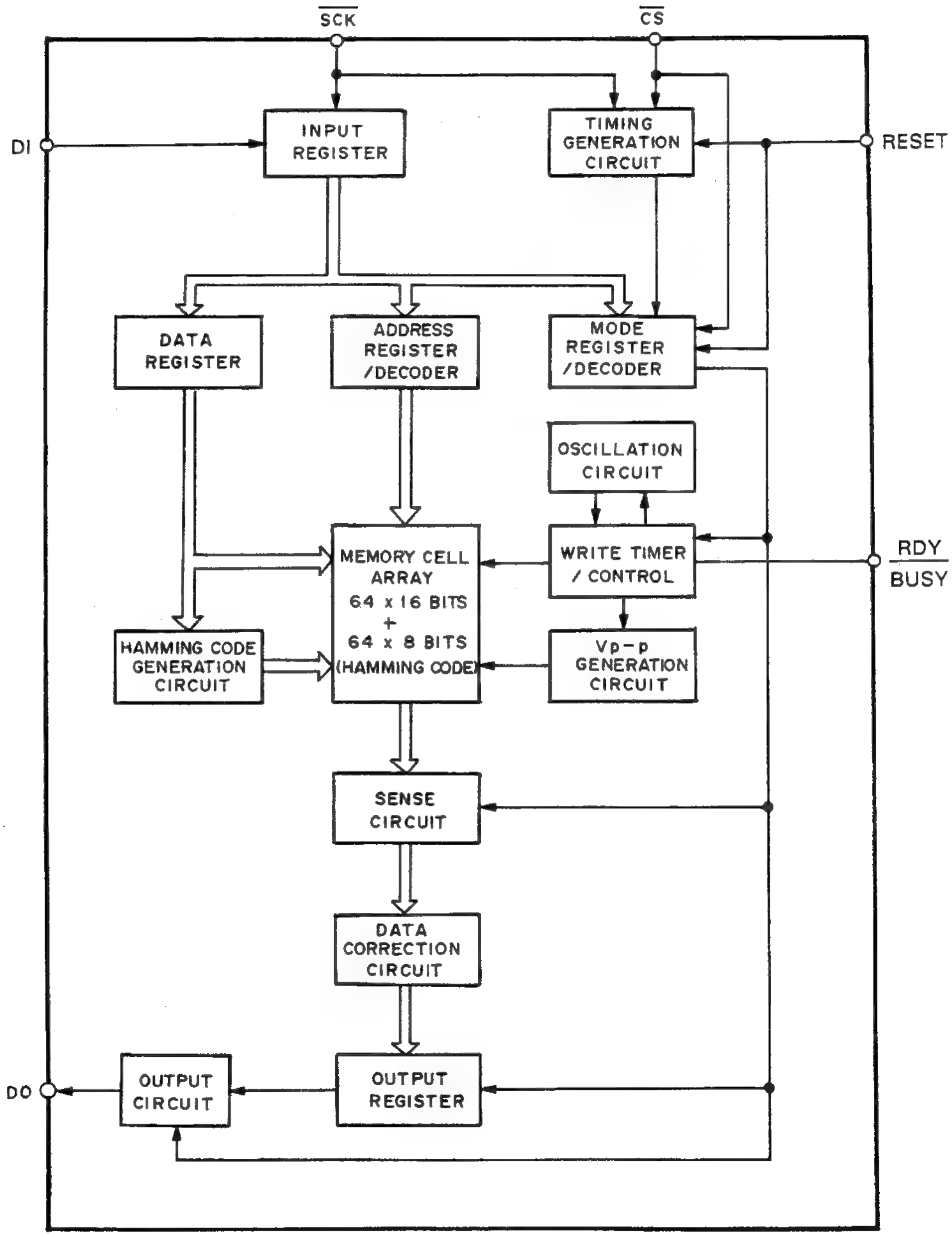


6.8 M6M80011L: IC15 (DTMC assembly)

- **Pin Connections**

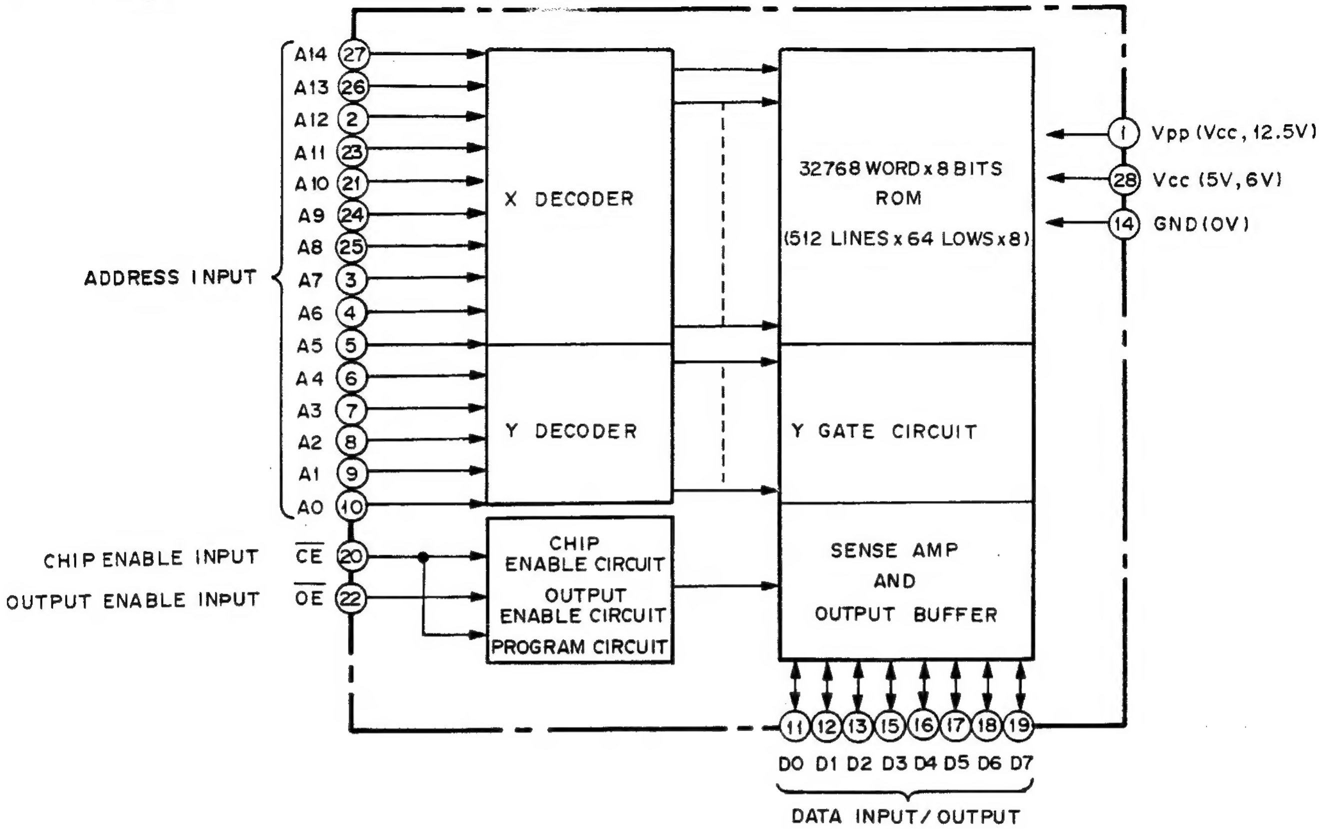


- **Block Diagram**



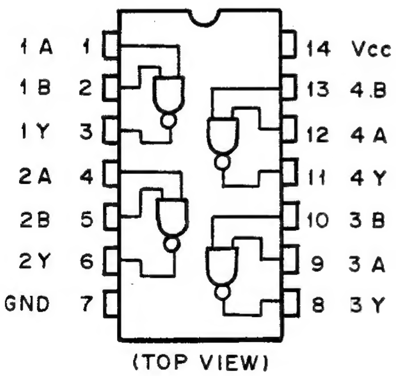
6.9 PROGRAM EPROM (DYW1035, DYW1036): IC9, IC10

• **Block Diagram**



6.10 TC74HC00AP

• **Pin Functions**

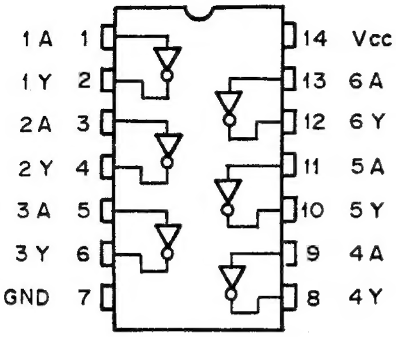


• **True Table**

A	B	Y
L	L	H
L	H	H
H	L	H
H	H	L

6.11 TC74HCT04AP

• **Pin Connections**



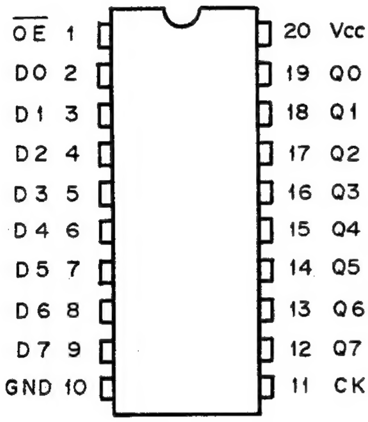
(TOP VIEW)

• **True Table**

A	Y
L	H
H	L

6.12 TC74HC574AF

• **Pin Connections**



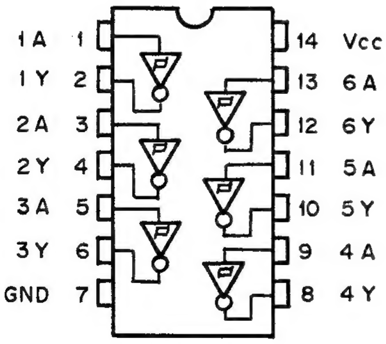
• **True Table**

INPUTS			OUTPUTS
$\overline{OE}$	CK	D	Q
H	X	X	Z
L	↓	X	Qn
L	↑	L	L
L	↑	H	H

X: Don't Care
Z: High-impedance
Qn: No change

6.13 TC74HC14AP

• **Pin Connectoins**



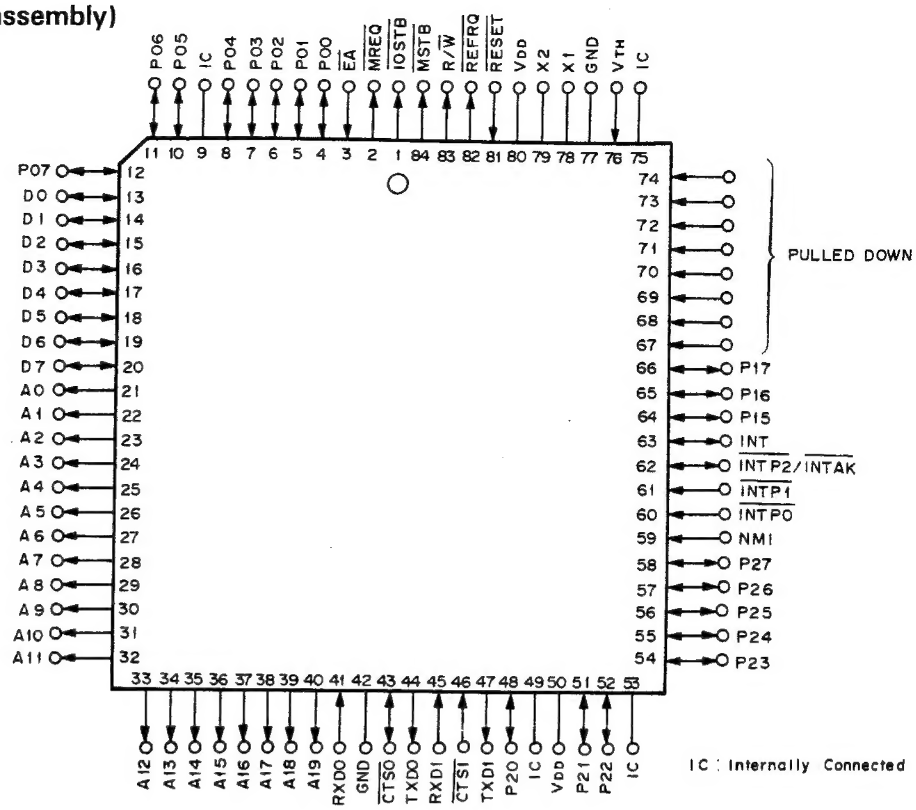
(TOP VIEW)

• **True Table**

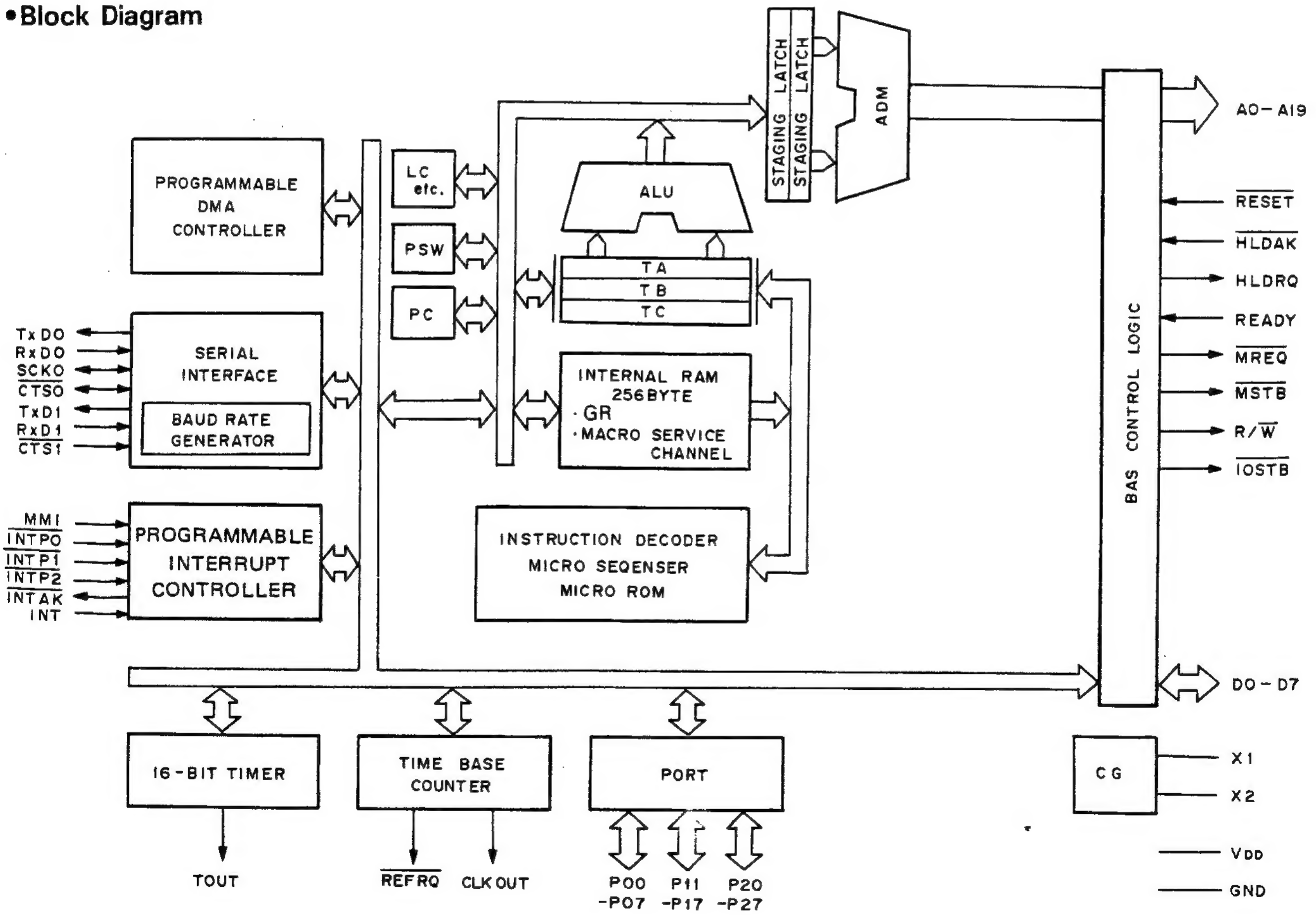
A	Y
L	H
H	L

6.14 μPD70320L: IC7 (DSCO assembly)

• **Pin Connections (Top View)**



• **Block Diagram**



• Pin Functions

Pin No.	Name	I/O	Function
1	IOSTB	OUT	I/O access strobe. (I/O Strobe)
2	$\overline{\text{MREQ}}$		Memory bus cycle start indication. (Memory Request)
3	EA	IN	External access.
4 – 8	P00 – P04	I/O	P00 – P04: Parallel data bus for communication with PD2021.
9	I.C.	–	Internally connected
10 – 12	P05 – P07	I/O	P05 – P07: Parallel data bus for communication with PD2021.
13 – 20	D0 – D7		8-bit data bus.
21 – 40	A0 – A19	OUT	Address bus.
41	R_XD0	IN	Serial data. Receive data 0
42	GND	–	GND pin
43	$\overline{\text{CTS0}}$	I/O	Asynchronous mode: Transmission indication input. I/O interface mode: Receiving clock I/O.
44	T_XD0	OUT	Serial data. Transmit data 0
45	R_XD1	IN	Serial data. Receive data 1
46	$\overline{\text{CTS1}}$		Transmission indication input.
47	T_XD1	OUT	Serial data. Transmit data 1
48	P20	I/O	P20: Parallel data bus for communication with PDE024.
49	I.C.	–	Internally connected
50	V_DD		Positive power supply pin (connect both two pins).
51	P21	I/O	P21: Parrallel data bus for communication with PDE024.
52	P22		P22: Parallel data bus for communication with PDE024.
53	I.C.	–	Internally connected
54 – 58	P23 – P27	I/O	P23 – P27: Parallel data bus for communication with PDE024.
59	NMI (P10)	IN	Not usable as general-purpose port. (non-maskable interruption)
60 – 62	$\overline{\text{INTP0}}$ – $\overline{\text{INTP2}}$		Interruption request input. Interrupt from peripheral 0, 1, 2.
63	INT		INT, P15 – P17: Parallel data bus control signal for communication with PD2021.
64 – 66	P15 – P17	I/O	
67 – 74	PT0 – PT7	IN	Comparator input. (Pull down)
75	I.C.	–	Internally connected.
76	V_TH	IN	Comparator reference voltage.
77	GND	–	GND pin
78	X1		System clock oscillator crystal connection. (Out-of-phase clock input possible to X1, X2)
79	X2		
80	V_DD		
81	$\overline{\text{RESET}}$	IN	Chip reset.
82	$\overline{\text{REFRQ}}$	OUT	DRAM refresh pulse. (Refresh Request)
83	R/$\overline{\text{W}}$		Read cycle/write cycle indication. (Read/write Strobe)
84	$\overline{\text{MSTB}}$		Memory access strobe. (Memory Strobe)